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PEW76/86/96 M/B Schematics Document

AMD Danube Only UMA

AMD Champlain Processor with RS880M/SB820M

2010-07-20

LA6552P REV: 1.0

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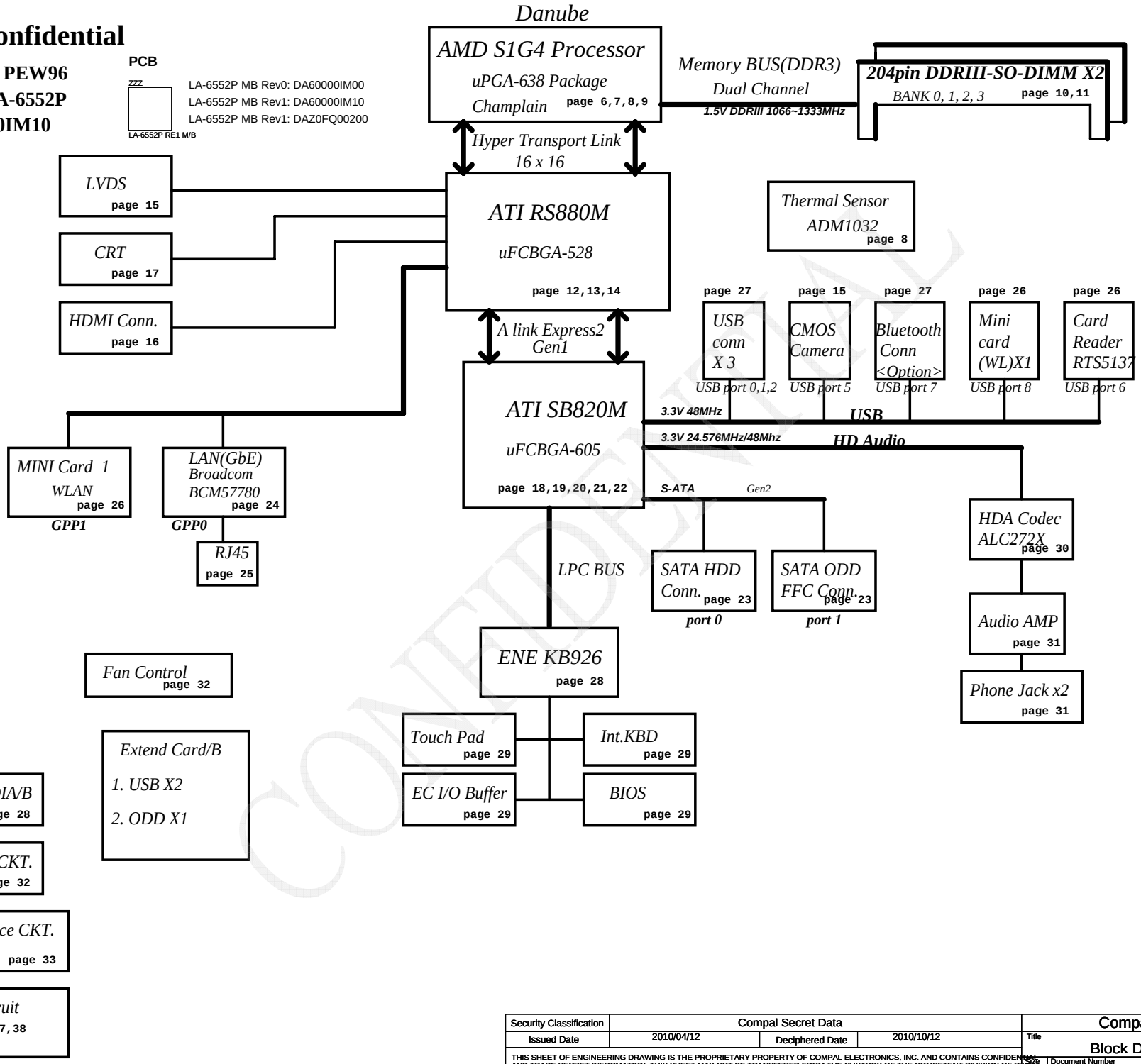
Model Name : PEW96
File Name : LA-6552P
P/N : DA60000IM10

PCB

ZZZ
LA-6552P RE1 M/B

LA-6552P MB Rev0: DA60000IM00
LA-6552P MB Rev1: DA60000IM10
LA-6552P MB Rev1: DAZ0FQ00200



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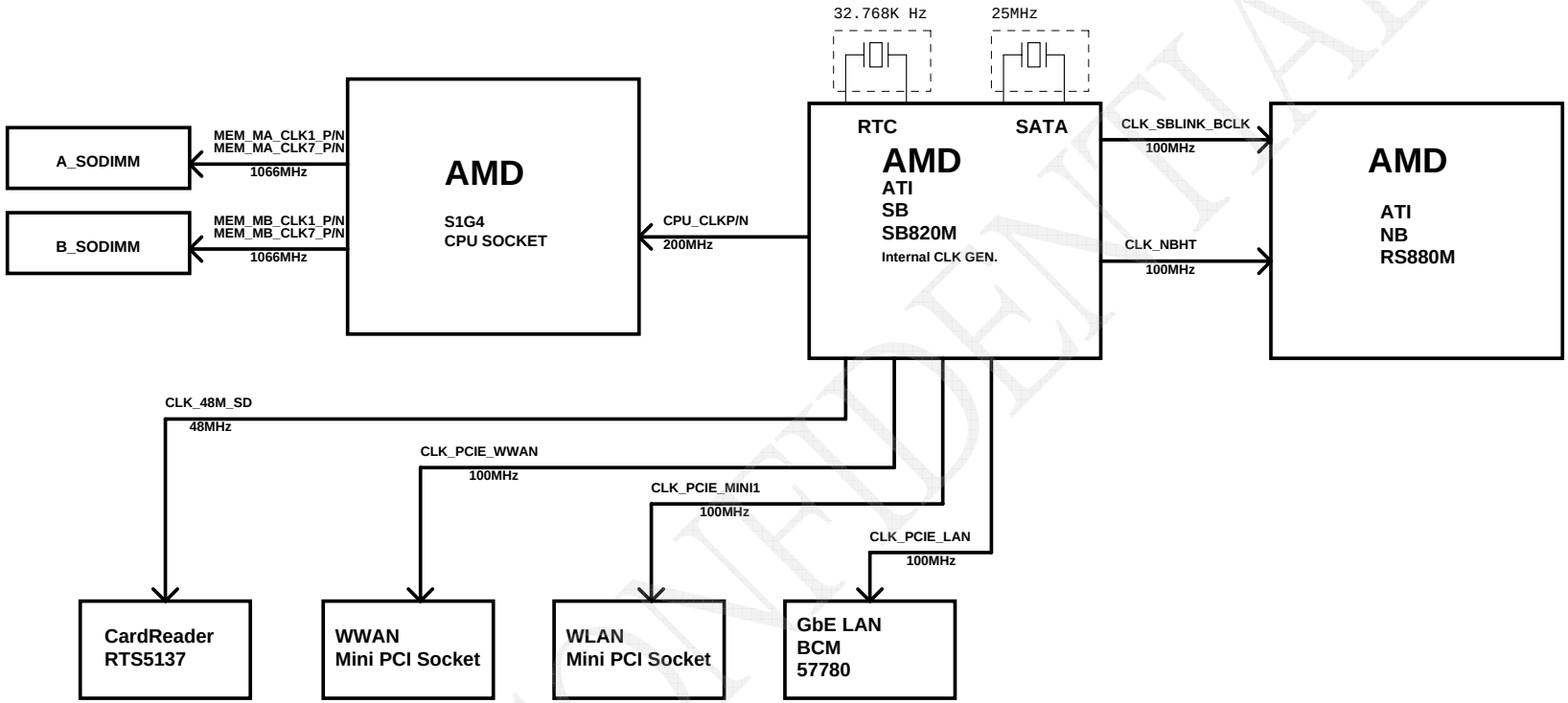

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU (1.375-1.5V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die Northbridge of CPU(0.8-1.1V)	ON	OFF	OFF
+CPU_VDDR	1.05V switched power rail	ON	OFF	OFF
+0.75V	0.75V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5VS	1.5V power rail for MINI Card	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

BOARD ID Table

Board ID	PCB Revision
0	EVT / PVT stage (w/ pach code)
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Bluetooth	BT@
Vari-Bright	VB@
No Vari-Bright	UNVB@
HDMI	HDMI@

EC SM Bus1 address

Device	Address	HEX
Smart Battery	0001 011X b	16H

EC SM Bus2 address

Device	Address	HEX
ADI ADM1032 (CPU)	1001 100X b	98H
SB-Temp Sensor		98H

Project ID Table

Board ID	PCB Revision
0	
1	PEW76/86/96
2	
3	
4	
5	
6	
7	

SB820 SM Bus 0 address

Device	Address	HEX
Clock Generator (SILEGO SLG8SP626)	1101 001Xb	D2
DDR DIMM1	1001 000Xb	90
DDR DIMM2	1001 010Xb	94
Mini card		

SB820 SM Bus 1 address

Device	Address

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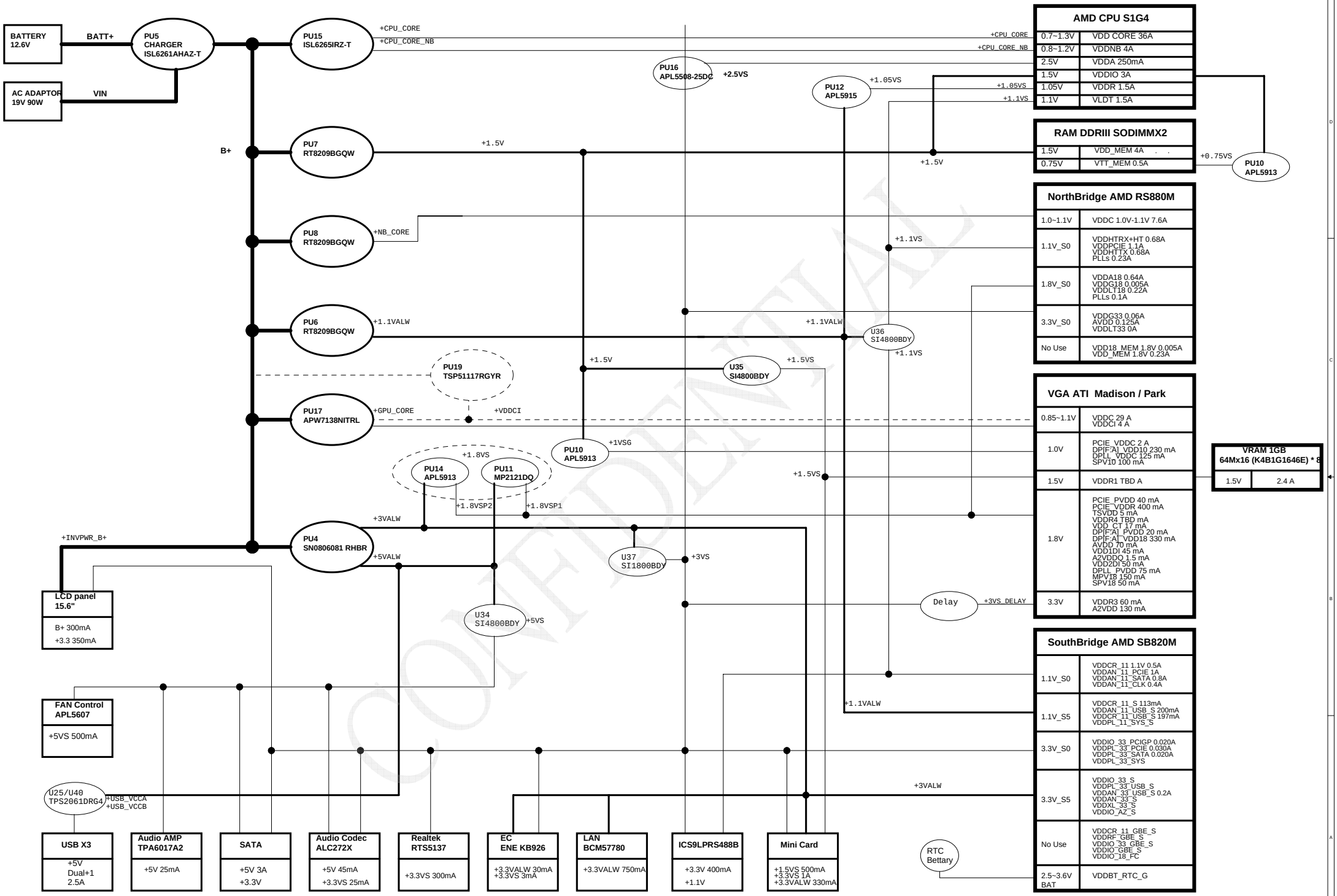

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Title: POWER DELIVERY CHART

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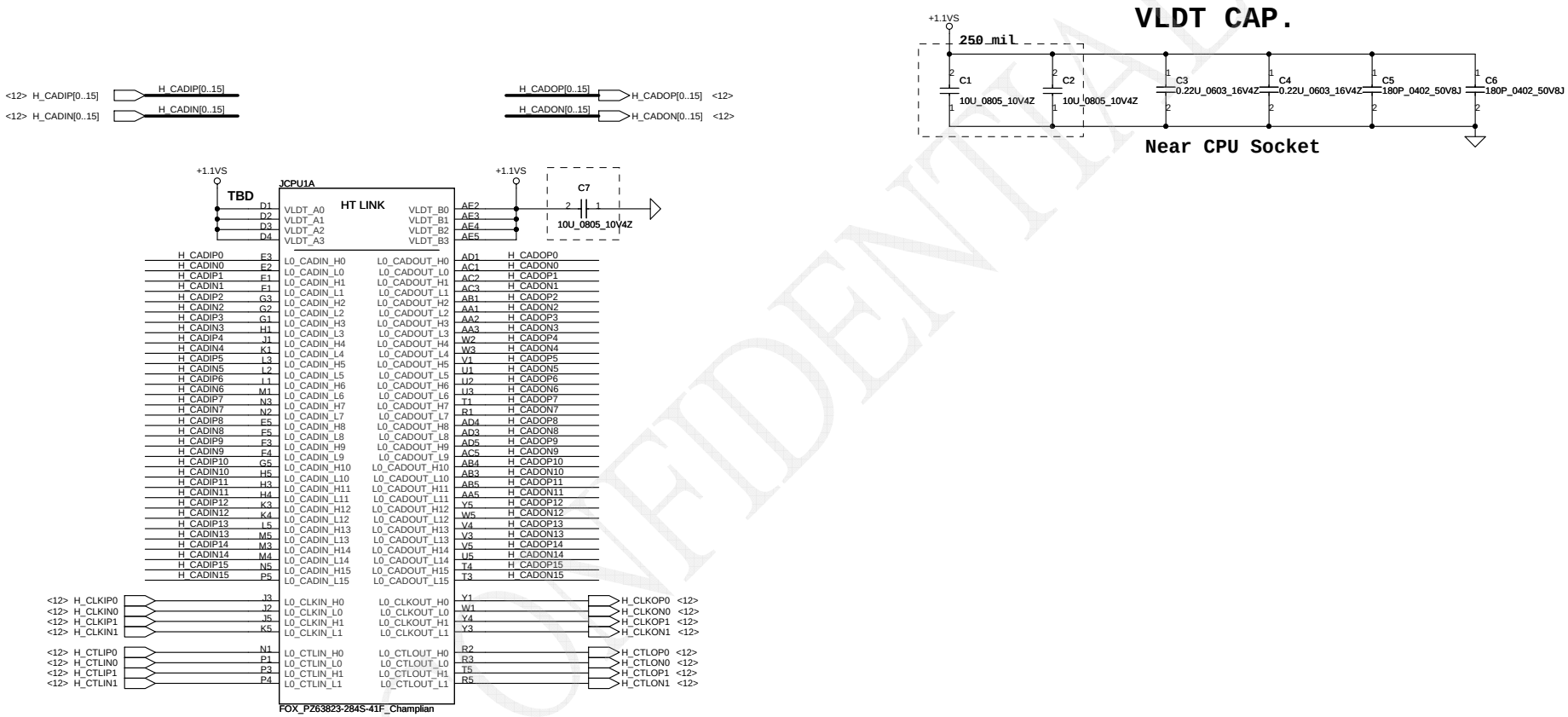

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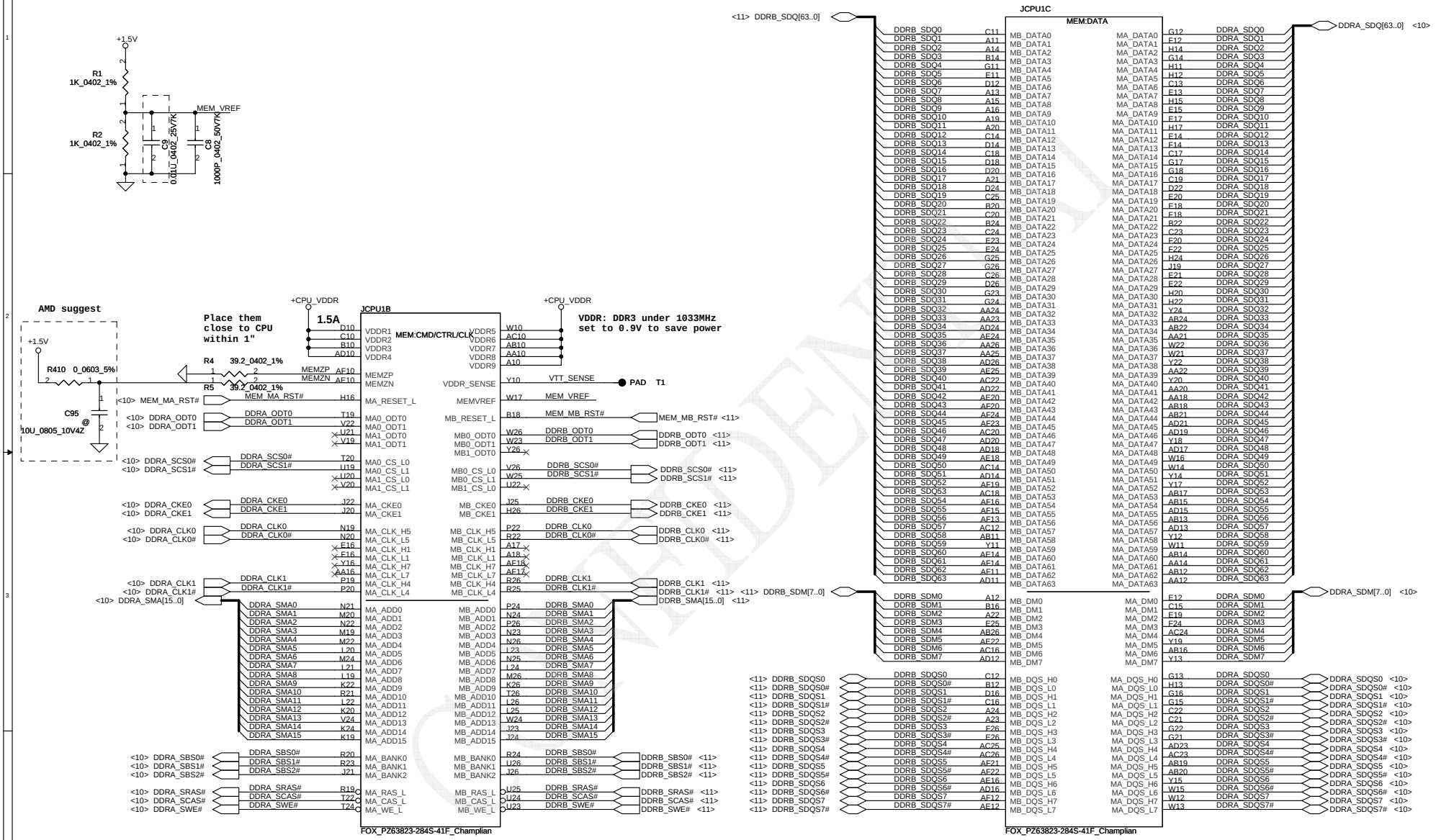
Processor DDR3 Memory Interface



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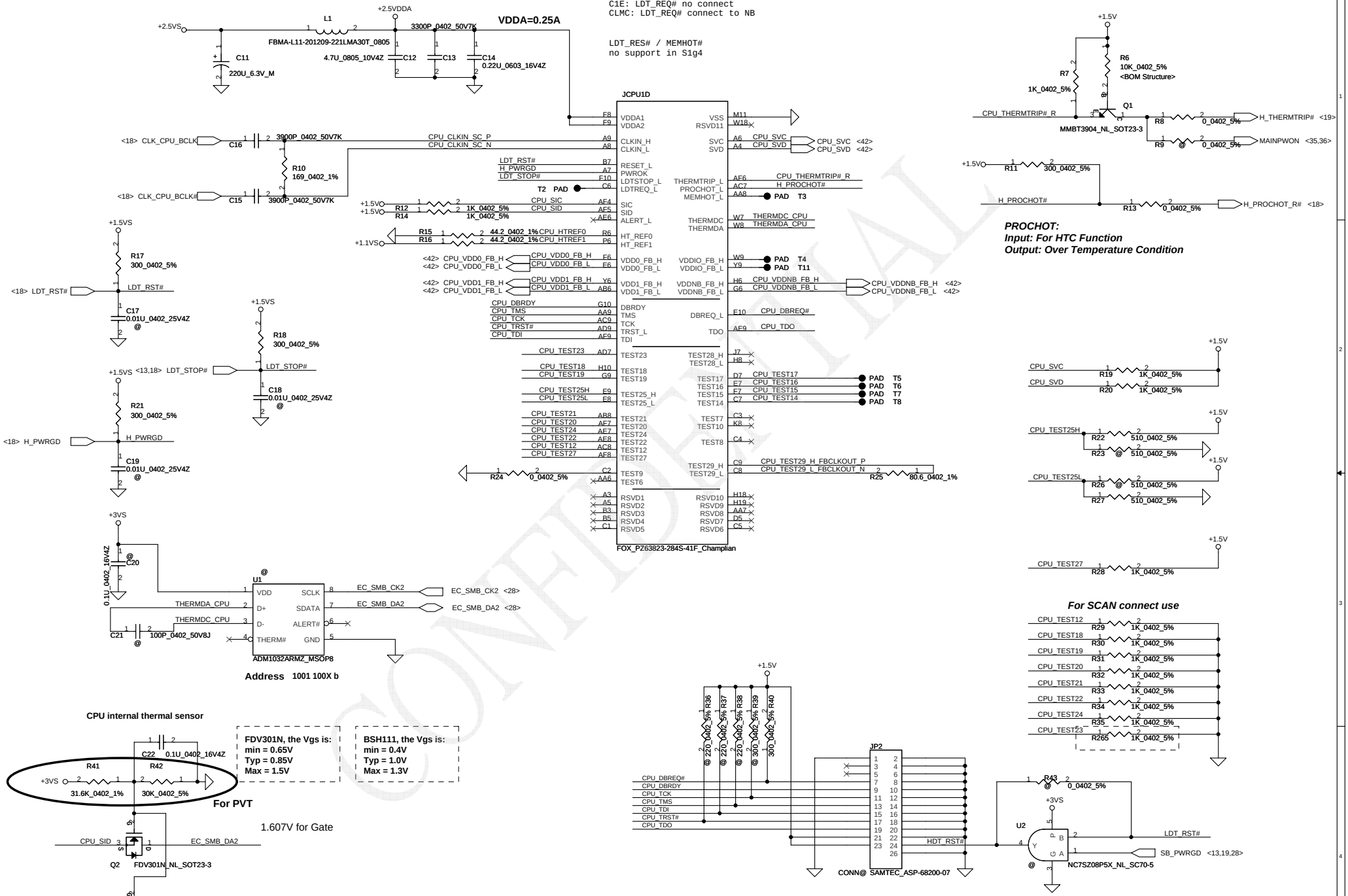

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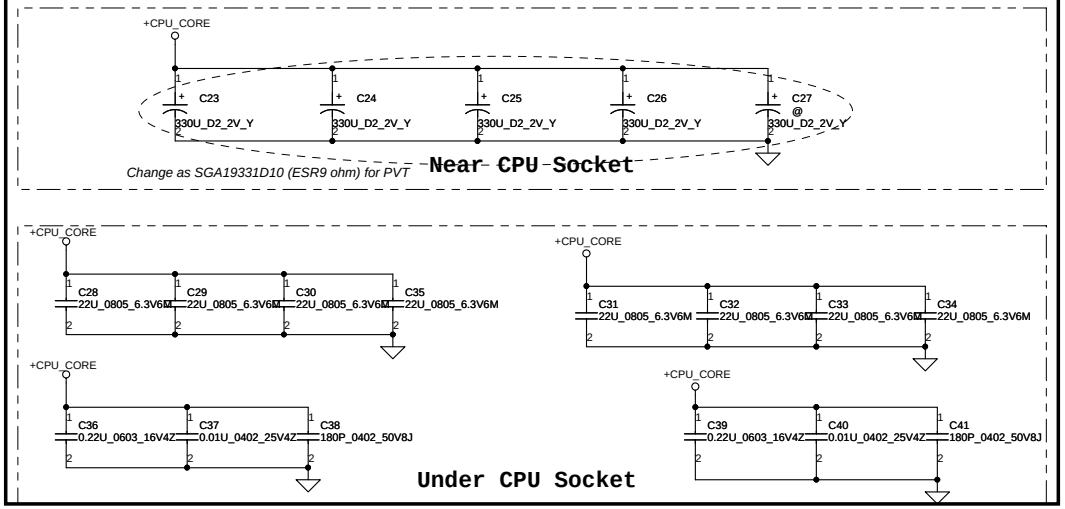
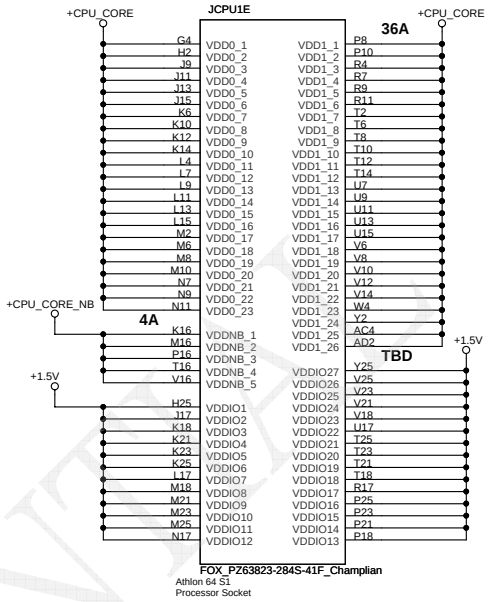
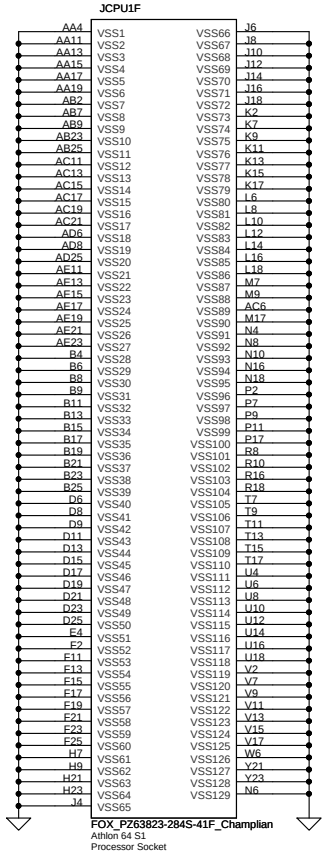
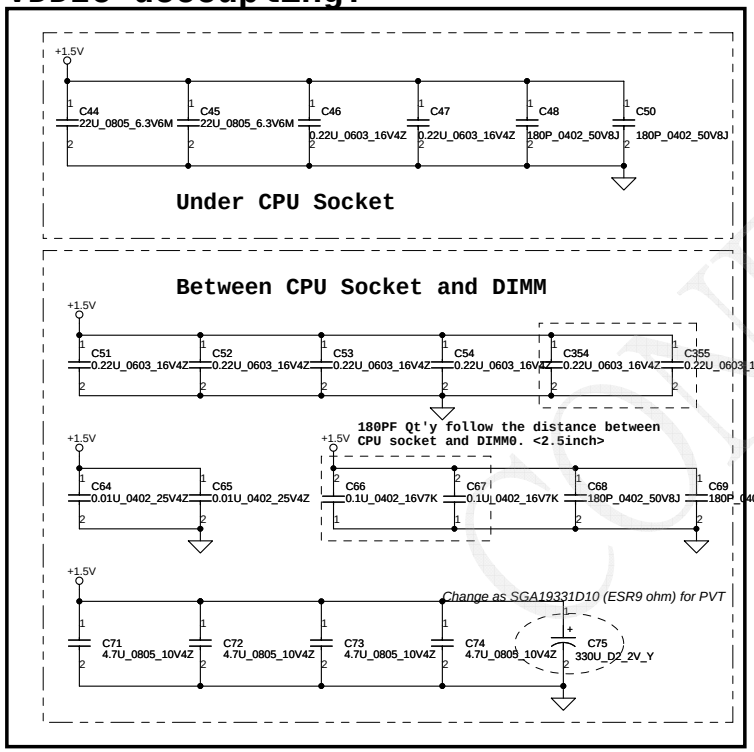
VDD(+CPU_CORE) decoupling.



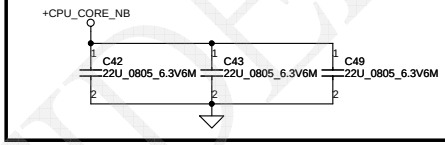




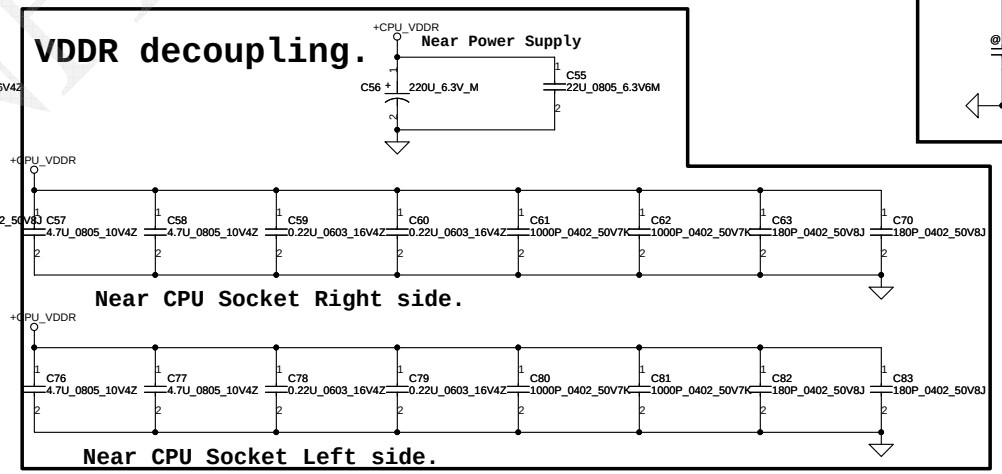
VDDIO decoupling.

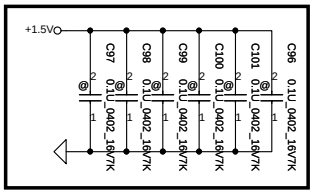


+CPU_CORE_NB decoupling.



VDDR decoupling.





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Title: AMD CPU S1G4 PWR & GND

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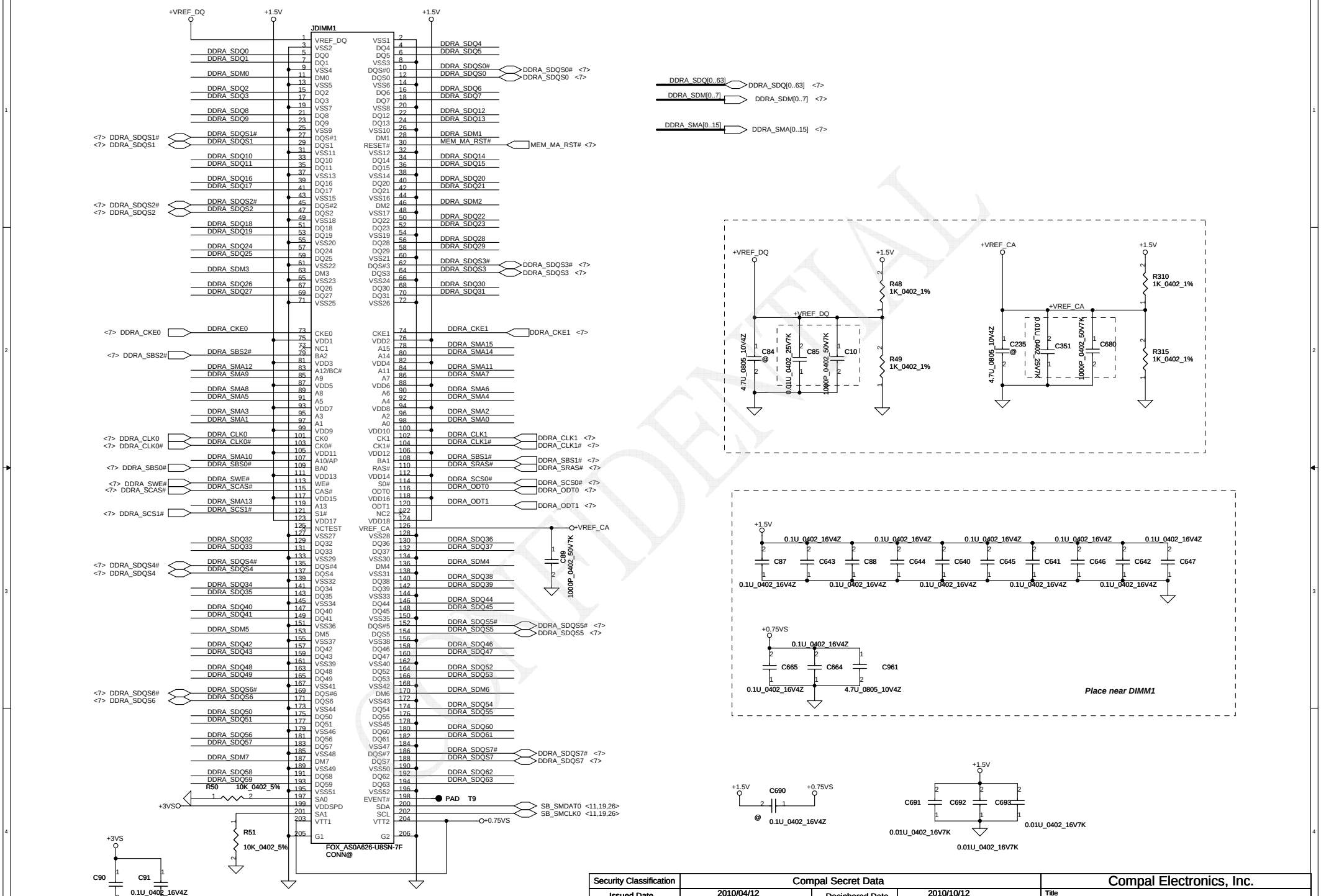

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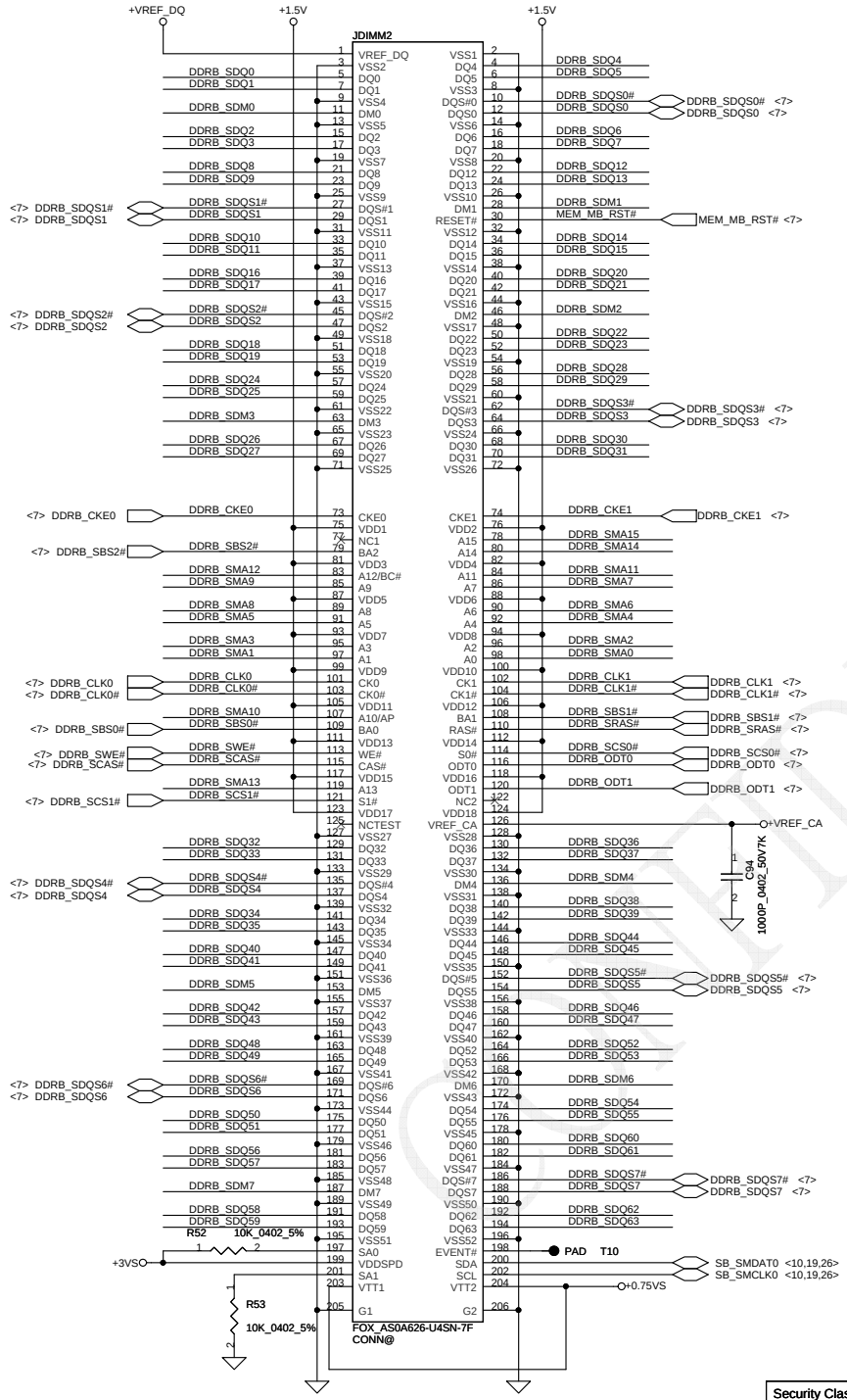

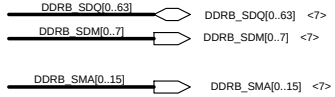

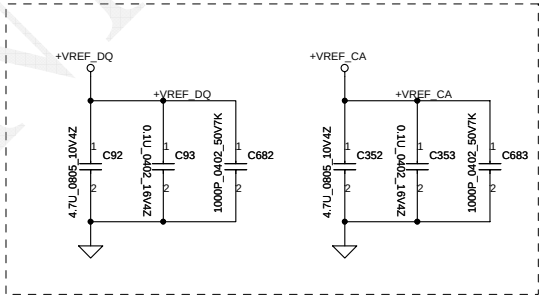

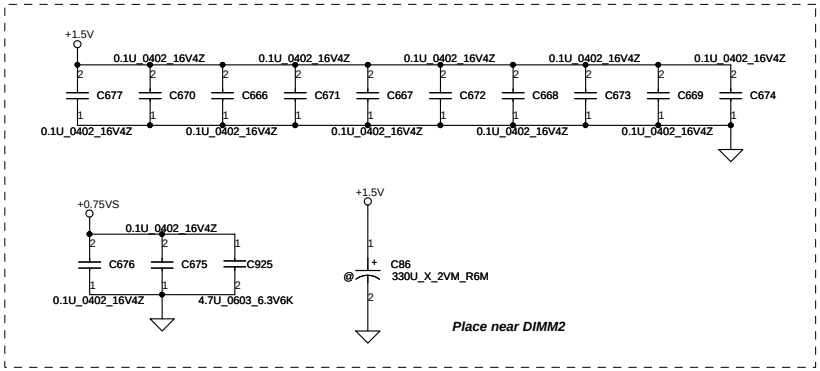

DIMM_B STD H:4mm

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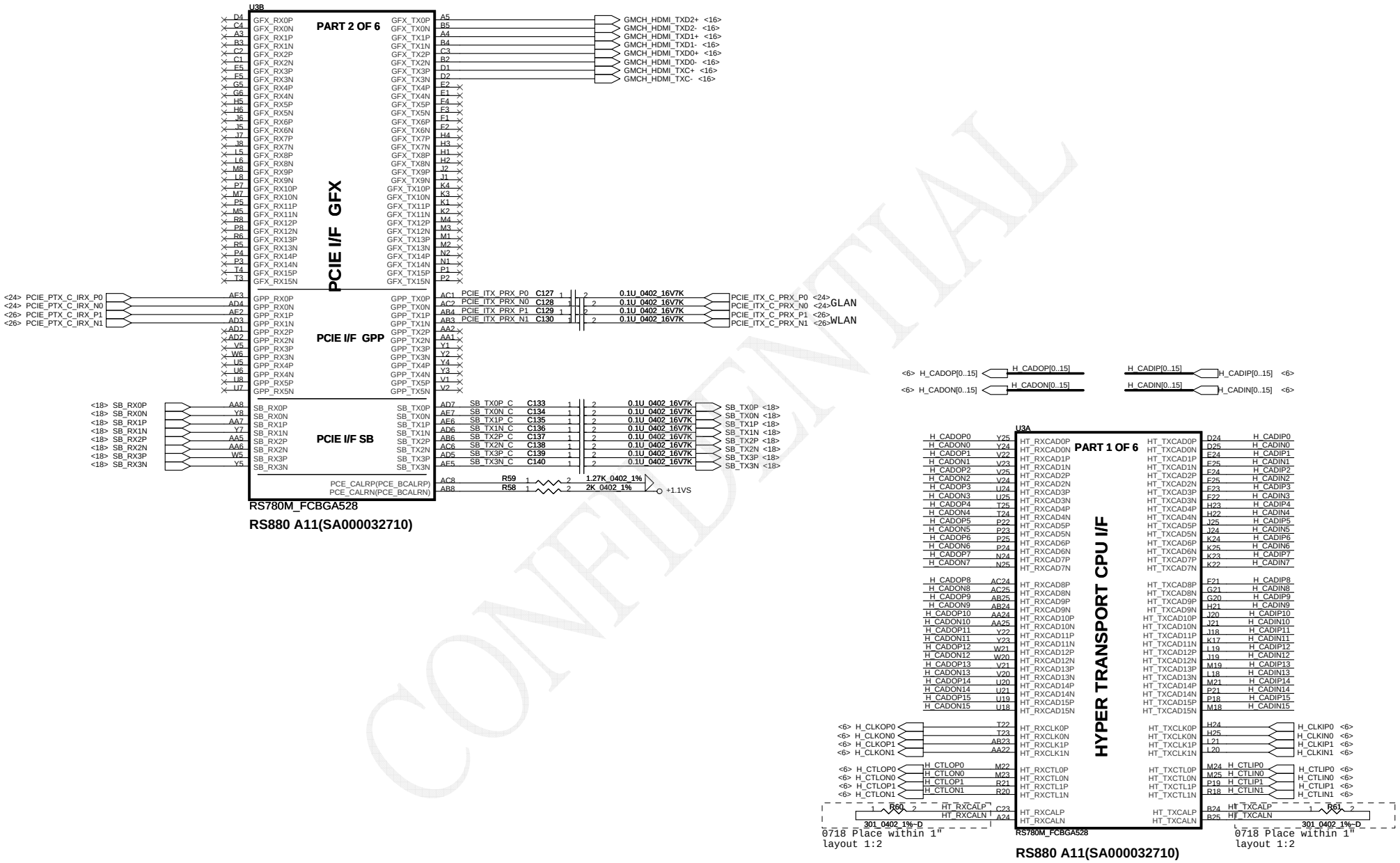

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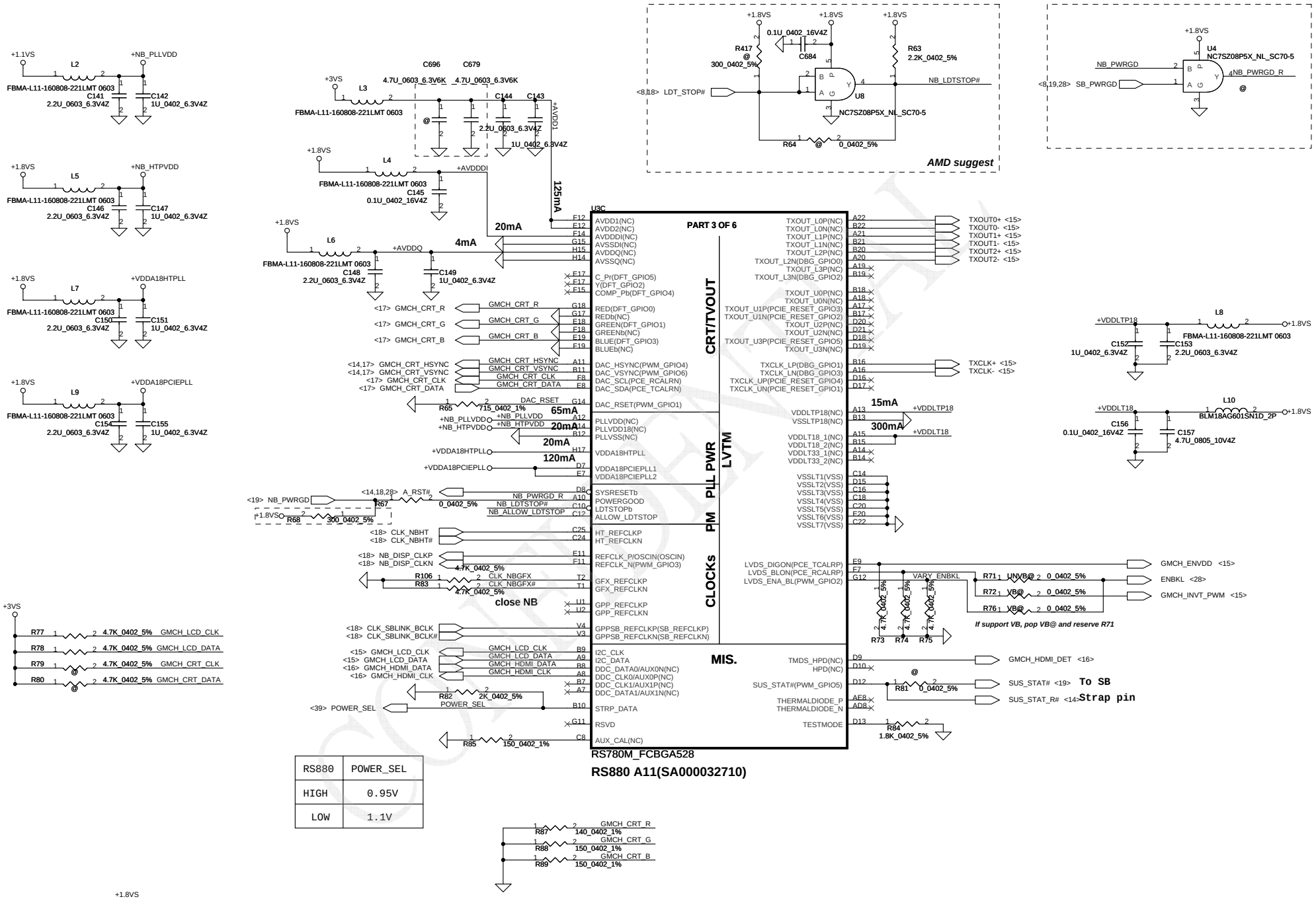

RS880	POWER_SEL
HIGH	0.95V
LOW	1.1V

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Compal Electronics, Inc.

Title: RS880 VEDIO/CLK GEN

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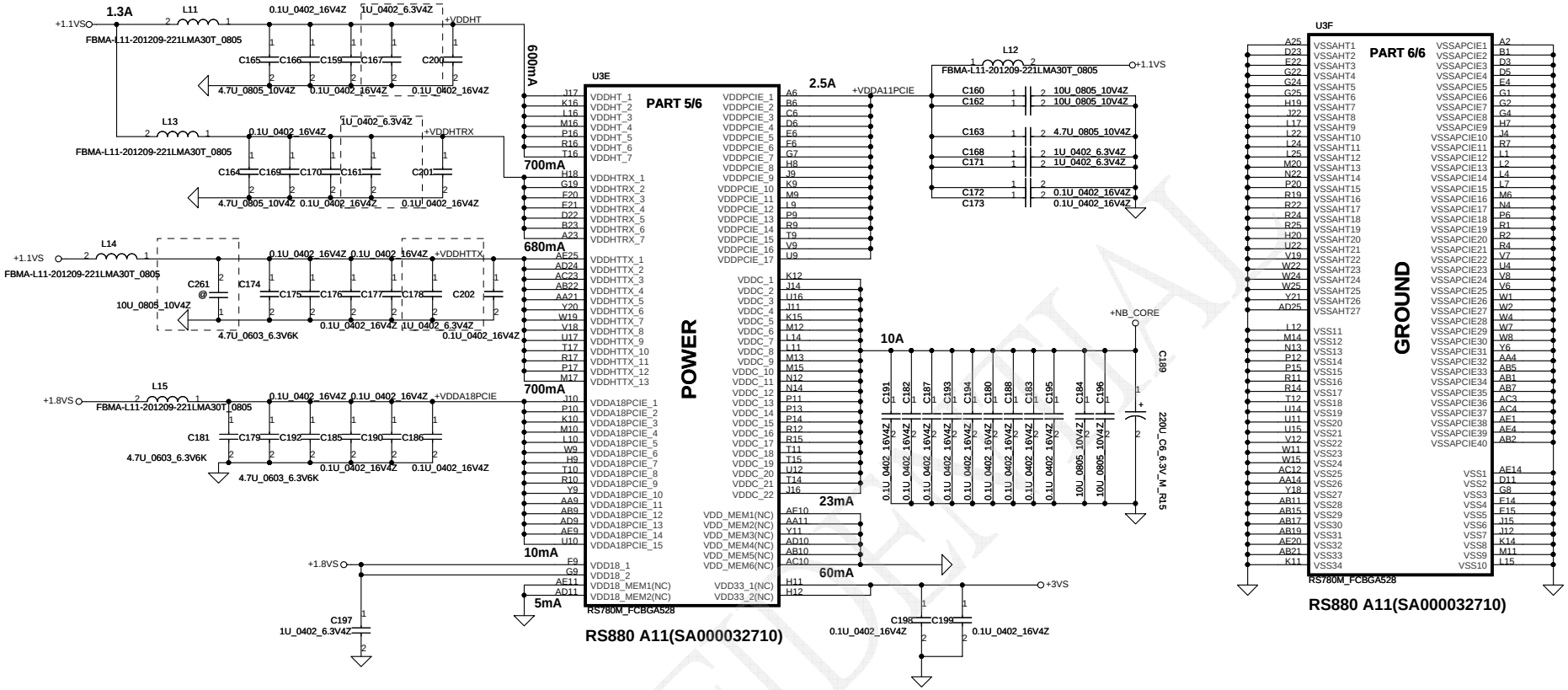
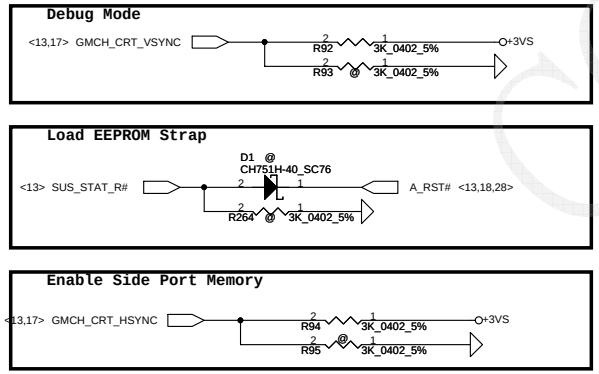


Side port and Strap setting



DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

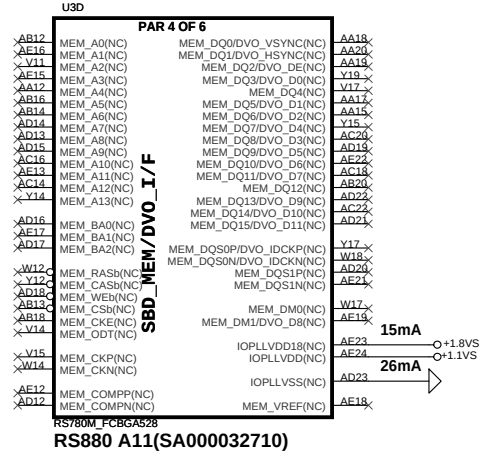
```
Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable
0 : Enable
```

DFT_GPIO1: LOAD_EEPROM_STRAPS

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
```

Enable Side Port Memory

```
RS880: HSYNC#
0:   Enable        Register Readback of strap:
1 :  Disable       NB_CLKCFG:CLK_TOP_SPARE_D[1]
```



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Size: Custom	Document Number: PEW/76/86/96 LA-6552P			Rev: B
Date: Thursday, July 22, 2010	Sheet 14 of 45			

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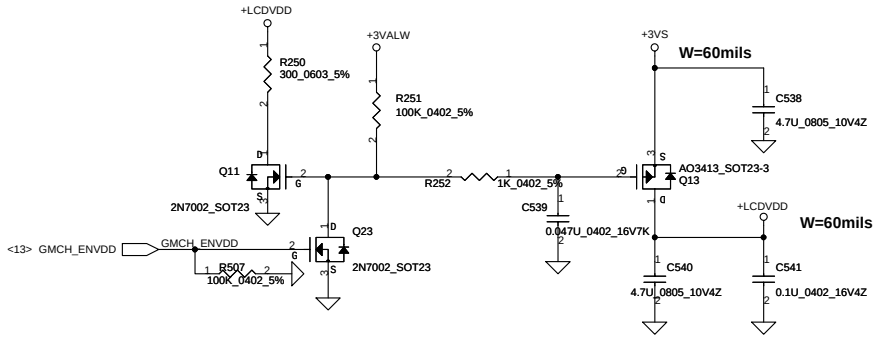
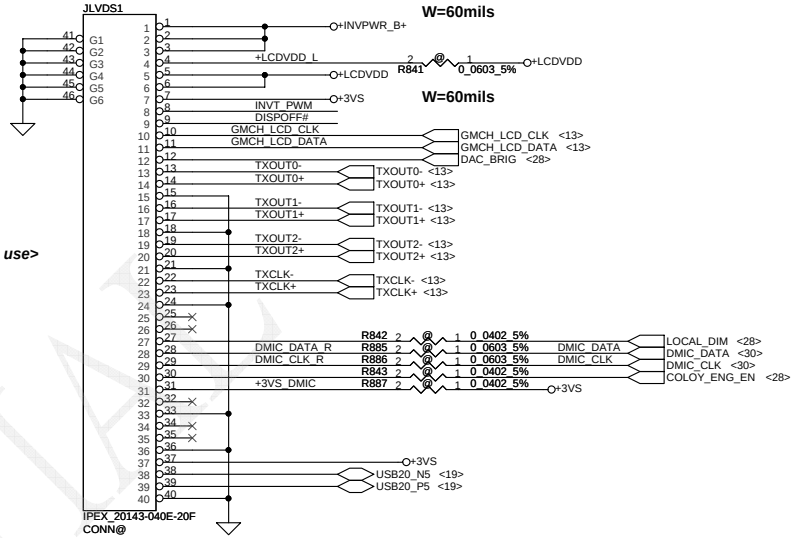
LCD POWER CIRCUIT



LCD/LED PANEL Conn.



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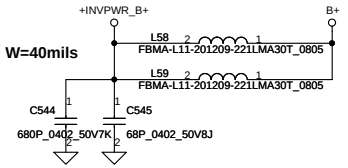

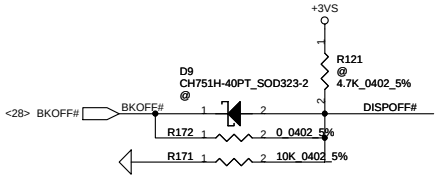

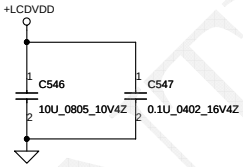

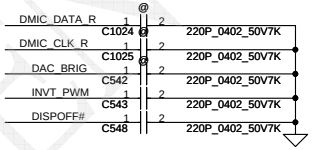

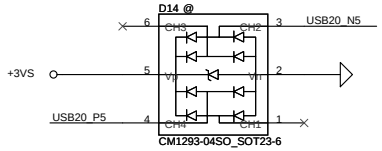

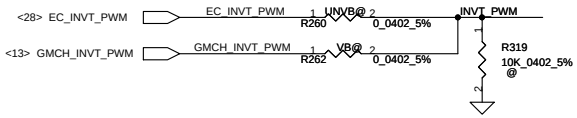

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				Date: Thursday, July 22, 2010; Sheet 15 of 45

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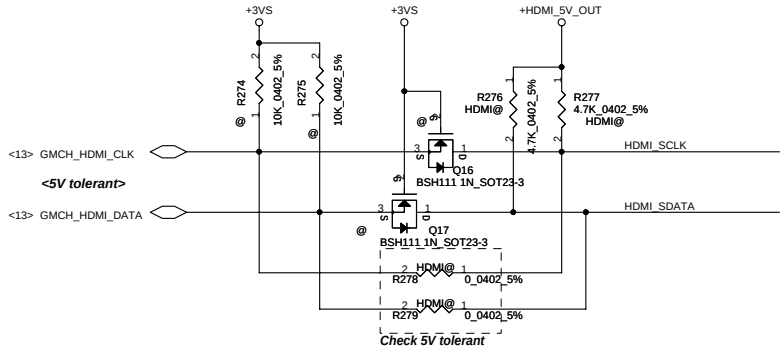

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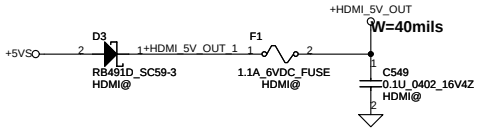

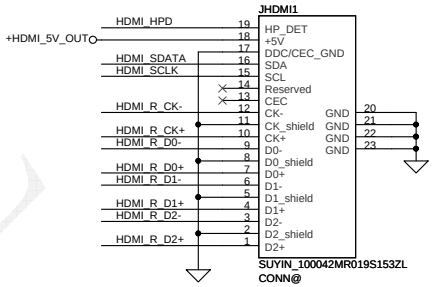

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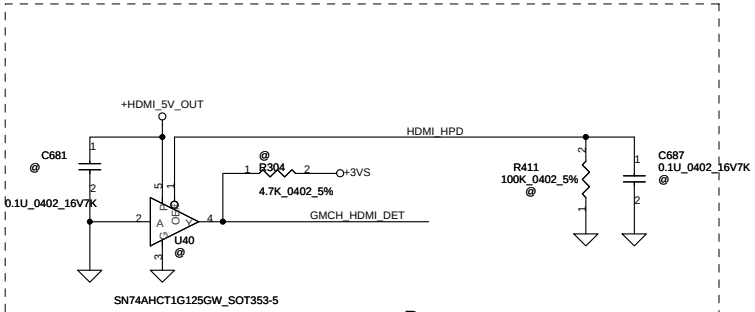
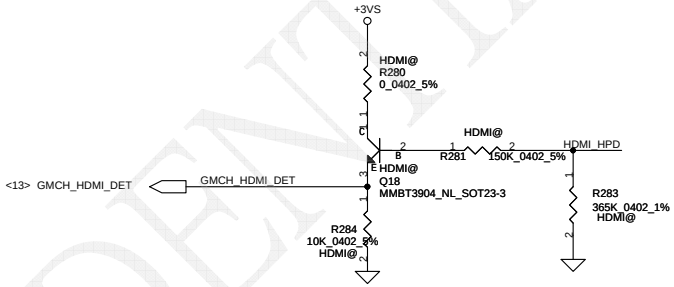
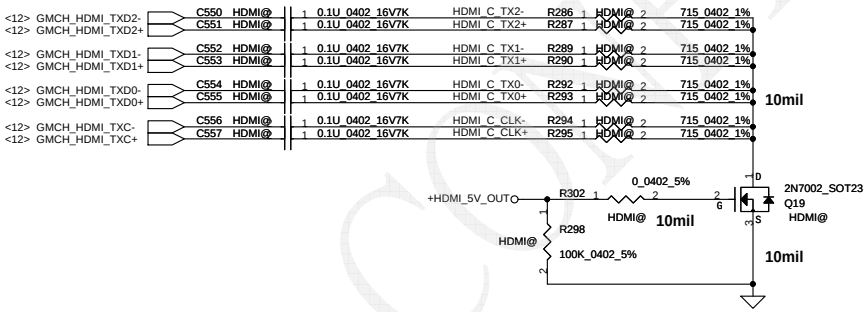


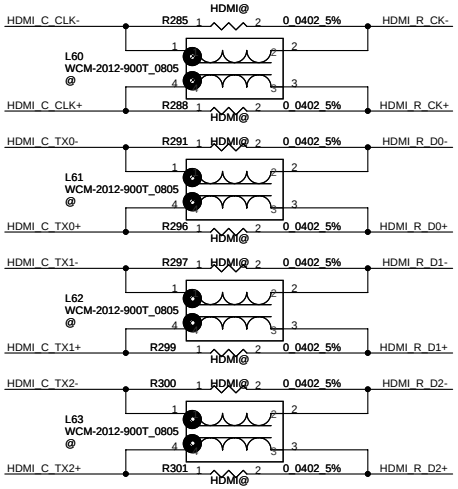
Reserve



UMA 715 ohm



Place closed to JHDMI1



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				Date: Thursday, July 22, 2010 / Sheet 16 of 45

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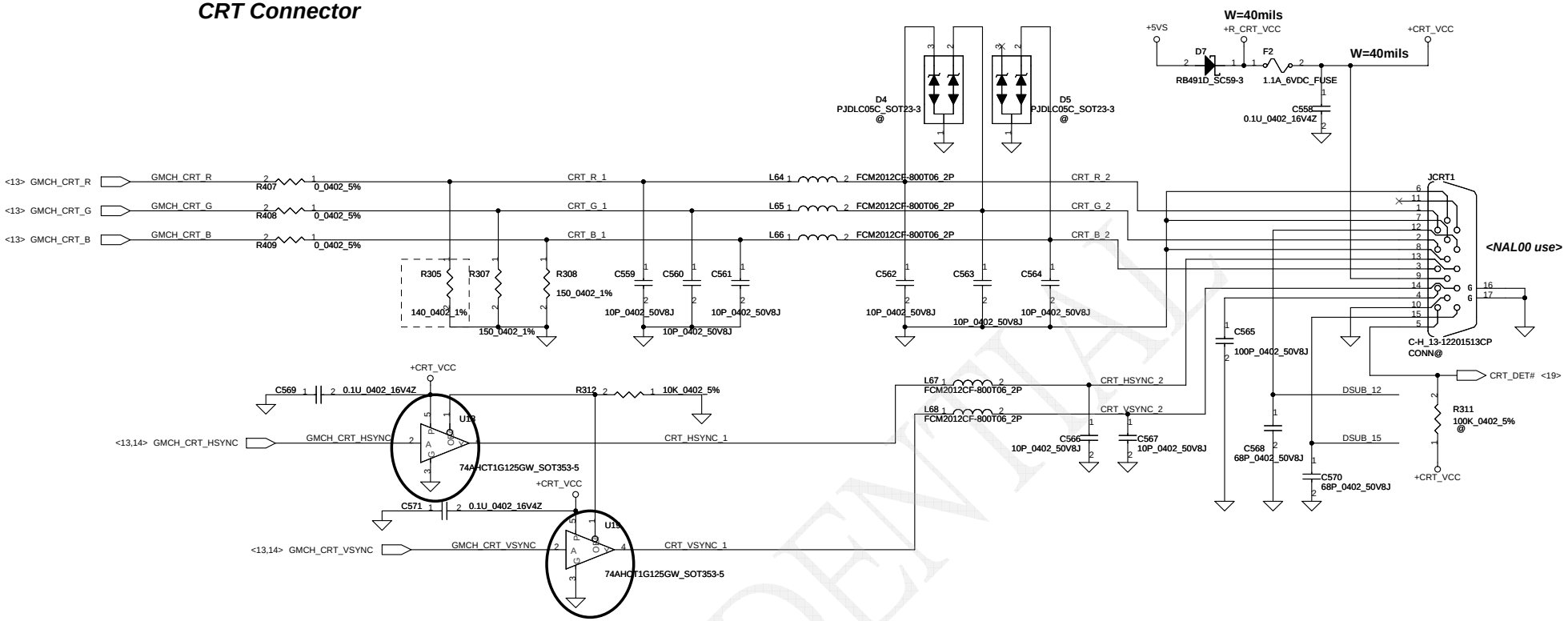
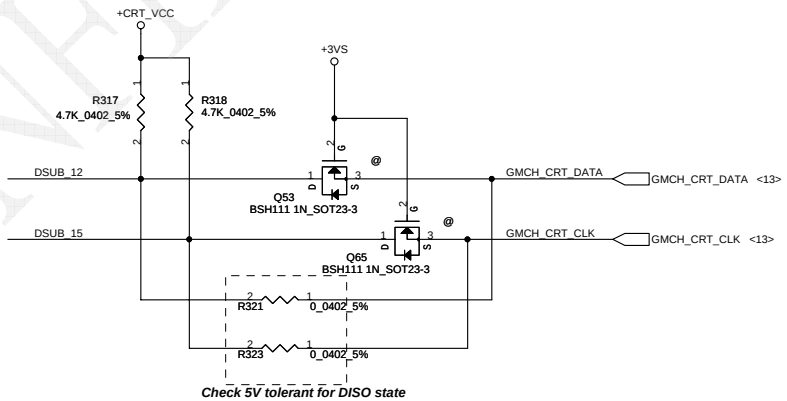
CRT Connector



Change as SA411250110

Close to Conn side



Check 5V tolerant for DISO state

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Issued Date	2010/04/12	Deciphered Date	2010/10/12	Title: CRT Connector
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				Date: Thursday, July 22, 2010; Sheet 17 of 45

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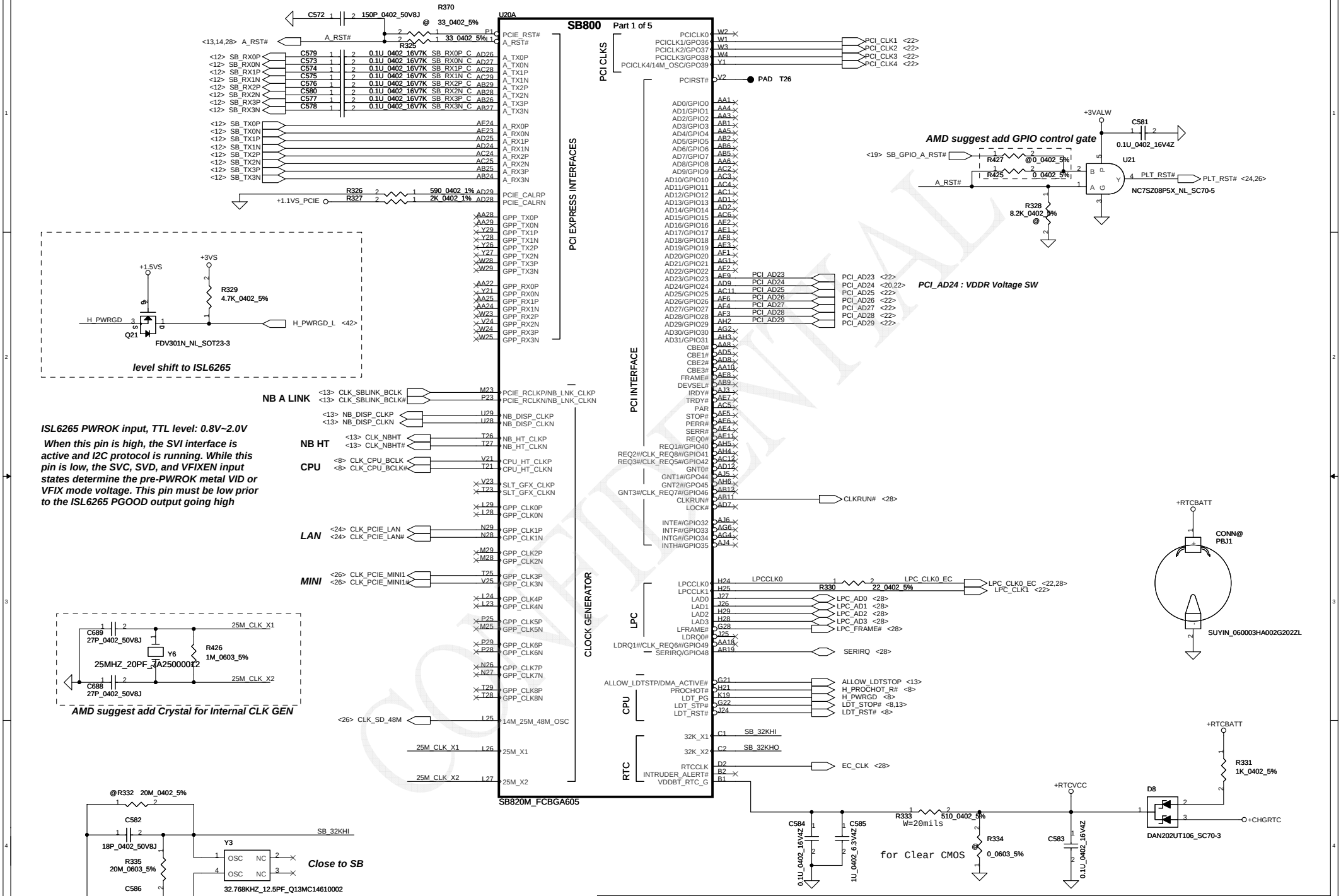

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/04/12	Deciphered Date	2010/10/12	Title: SB820-PCIE/PCI/ACPI/LPC/RTC
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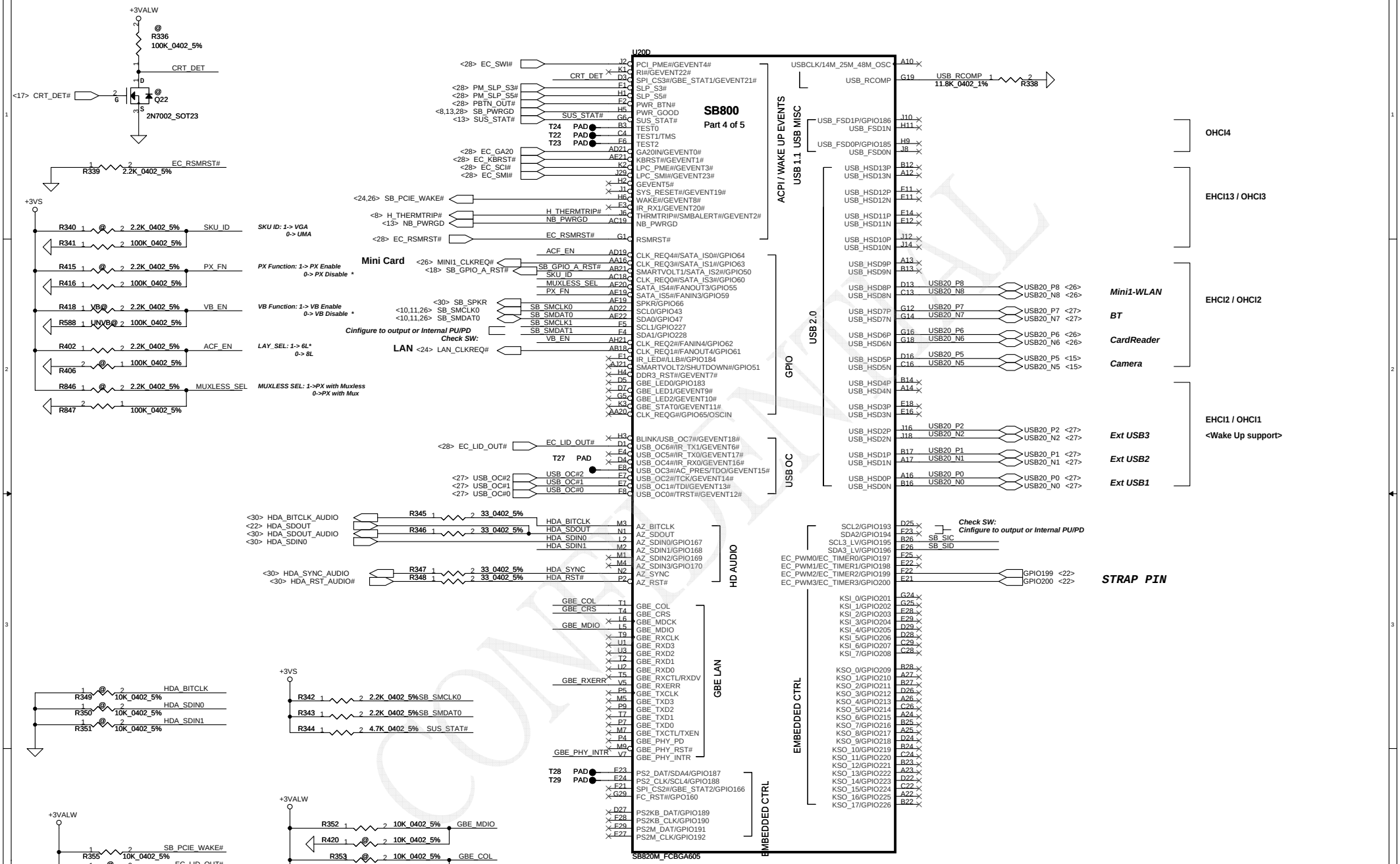
				Date: Thursday, July 22, 2010; Sheet 18 of 45



Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/10/12

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Compal Electronics, Inc.

Title: SB820 USB/HD audio

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Date: Thursday, July 22, 2010 | Sheet 19 of 45

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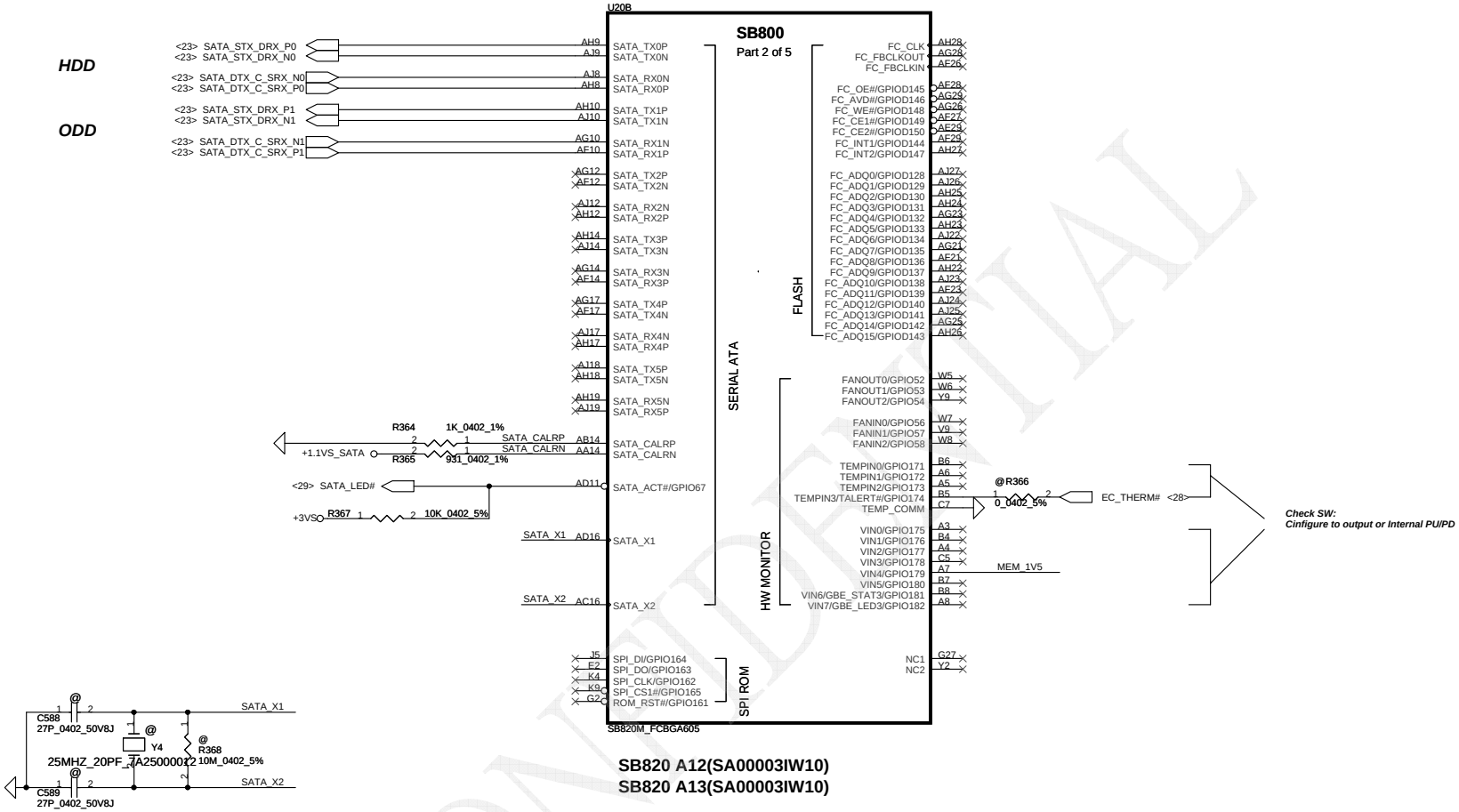
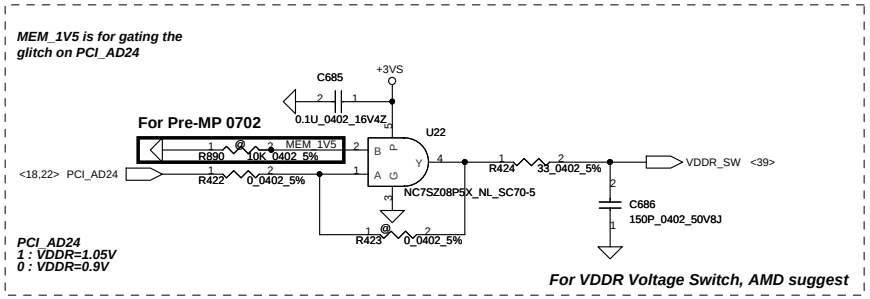


SB820 A12(SA00003IW10)
SB820 A13(SA00003IW10)



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/04/12	Deciphered Date	2010/10/12	Title: SB820 SATA/IDE/SPI
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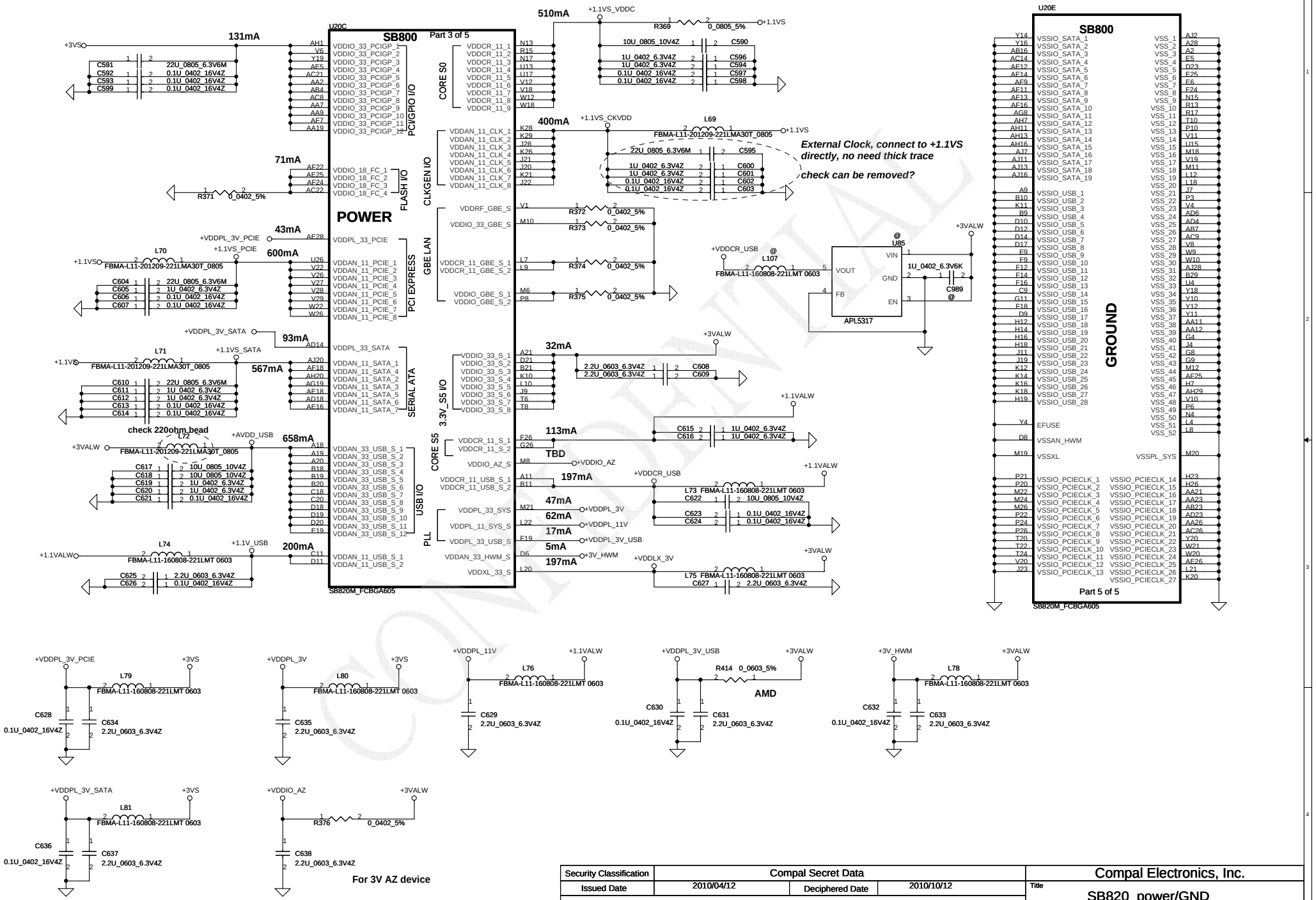

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/04/12	Deciphered Date	2010/10/12	Title: SB820 power/GND

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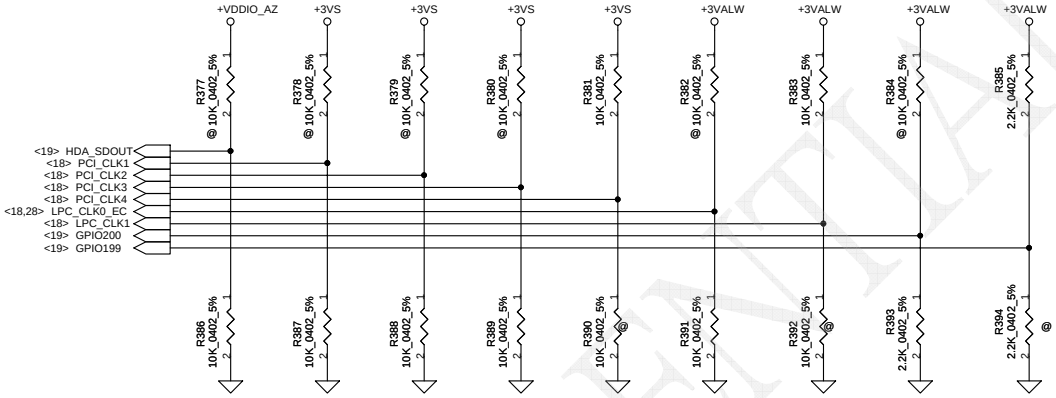
REQUIRED STRAPS

Check Internal PU/PD

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LCP_CLK1		GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	Inter CLK Gen Mode Enable	EC ENABLE	CLOCKGEN ENABLE		H,H = Reserved H,L = SPI ROM **L,H = LPC ROM (Default L,NC)** L,L = FWH ROM
PULL LOW	Performance MODE DEFAULT	FORCE PCIE GEN1 DEFAULT	WATCHDOG TIMER DISABLE DEFAULT	IGNORE DEBUG STRAP DEFAULT	Inter CLK Gen Mode Disable DEFAULT	EC DISABLE DEFAULT	CLOCKGEN DISABLE DEFAULT		



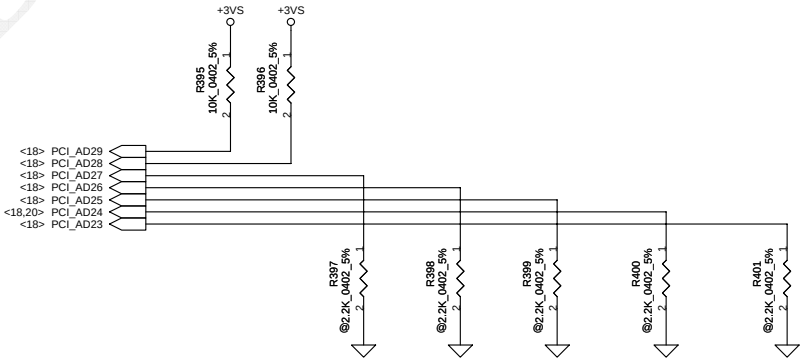
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

		PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH		USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW		BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Check AD29,AD28 strap function

check default



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			Date: Thursday, July 22, 2010; Sheet 22 of 45

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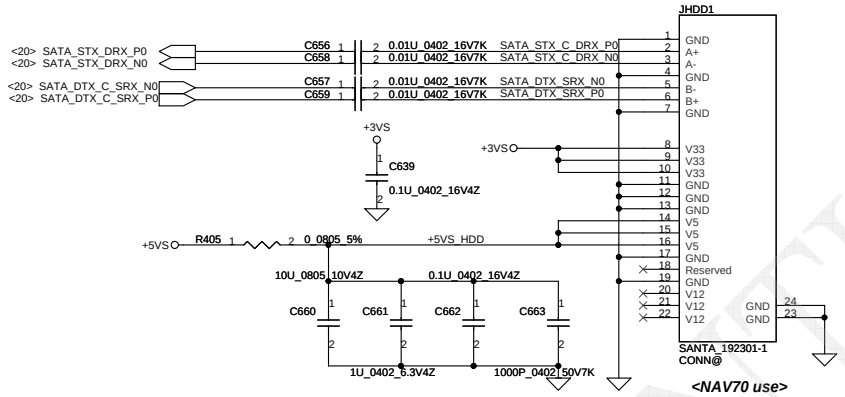
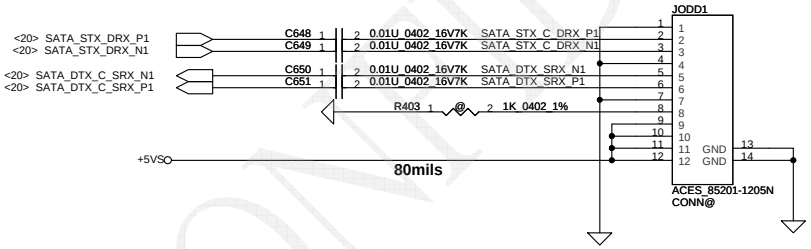
SATA HDD Conn.



SATA ODD FFC Conn.



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Issued Date	2010/04/12	Deciphered Date	2010/10/12	Title: HDD & ODD Connector
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				Date: Thursday, July 22, 2010; Sheet 23 of 45

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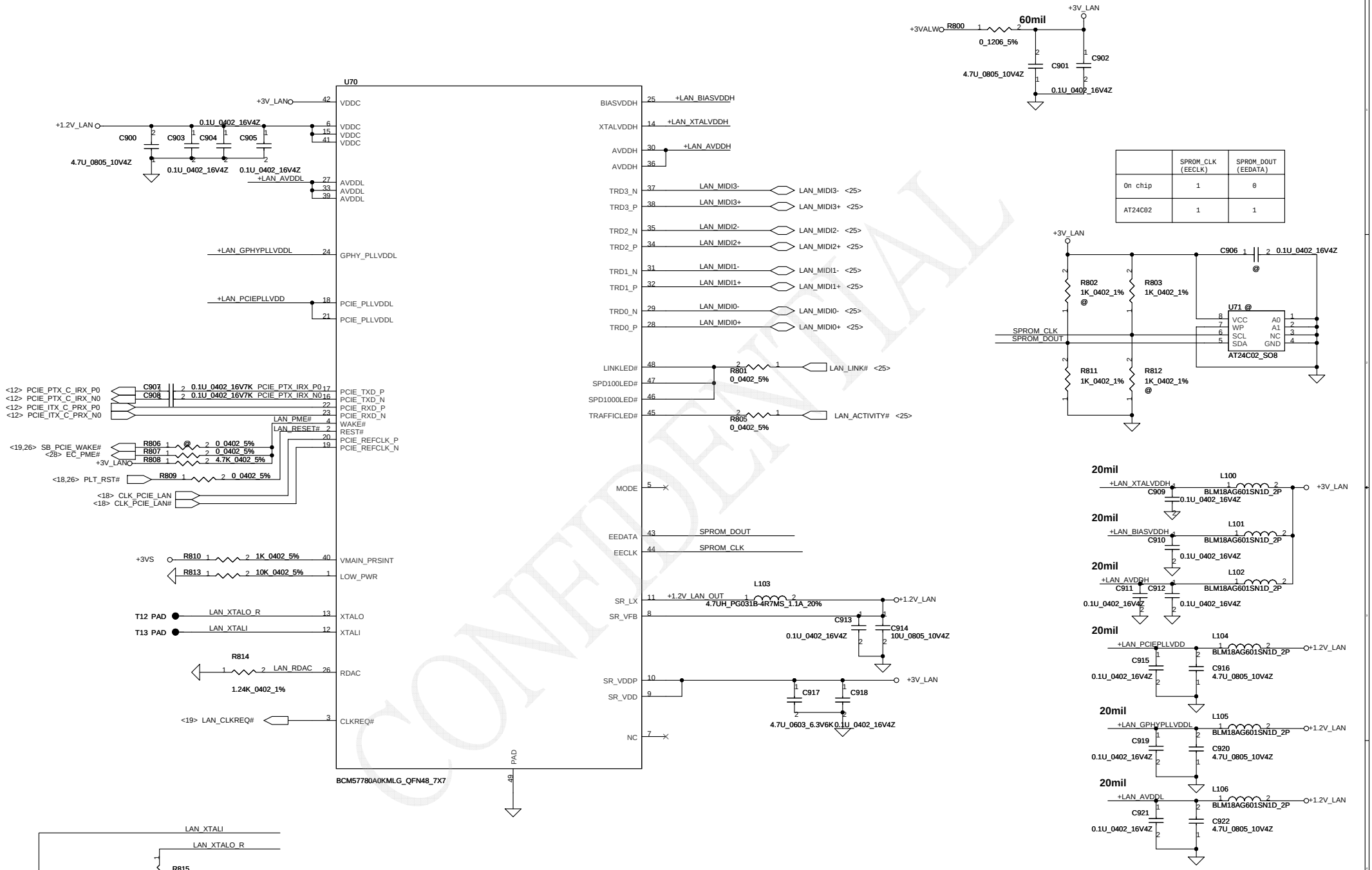

	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

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Security Classification	Compal Secret Data		
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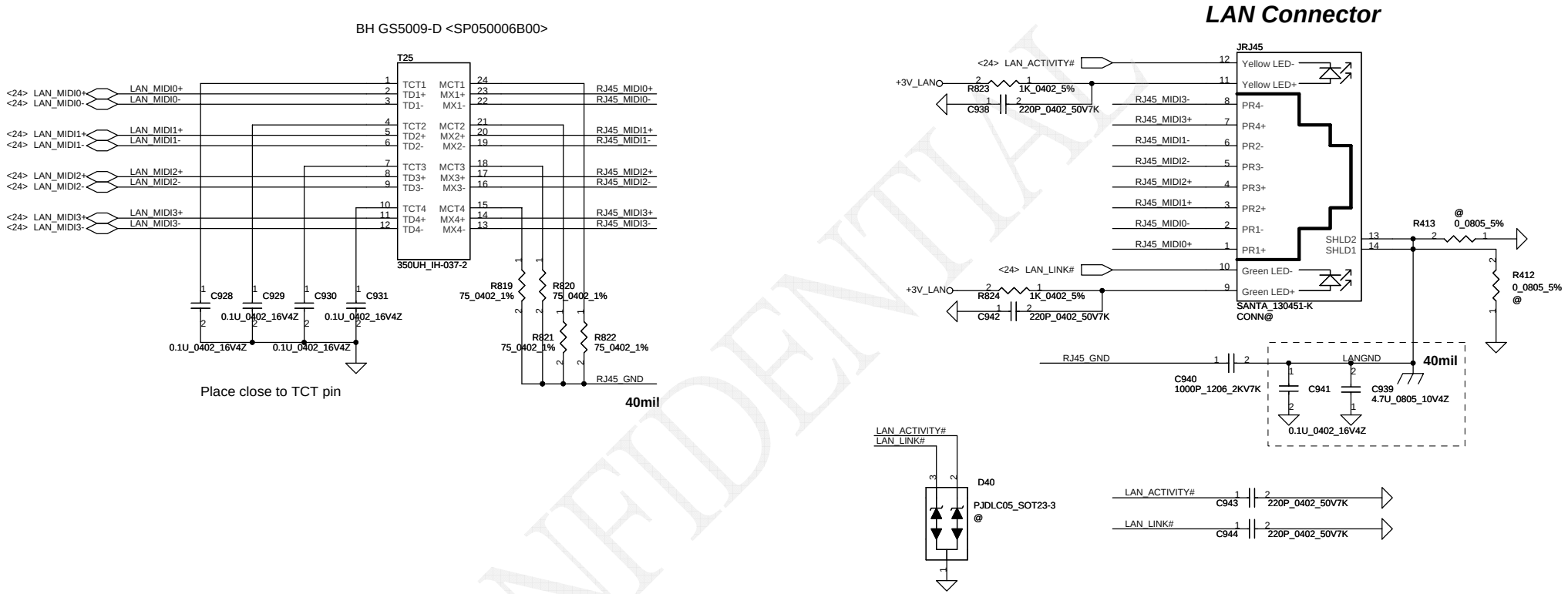
Compal Electronics, Inc.

Title: BROADCOM 57780

Size: Custom | Document Number: PEW/76/86/96 LA-6552P | Rev: B

Date: Thursday, July 22, 2010 | Sheet 24 of 45



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Issued Date	2010/04/12	Deciphered Date	2010/10/12	Title: LAN Magnetic & RJ45
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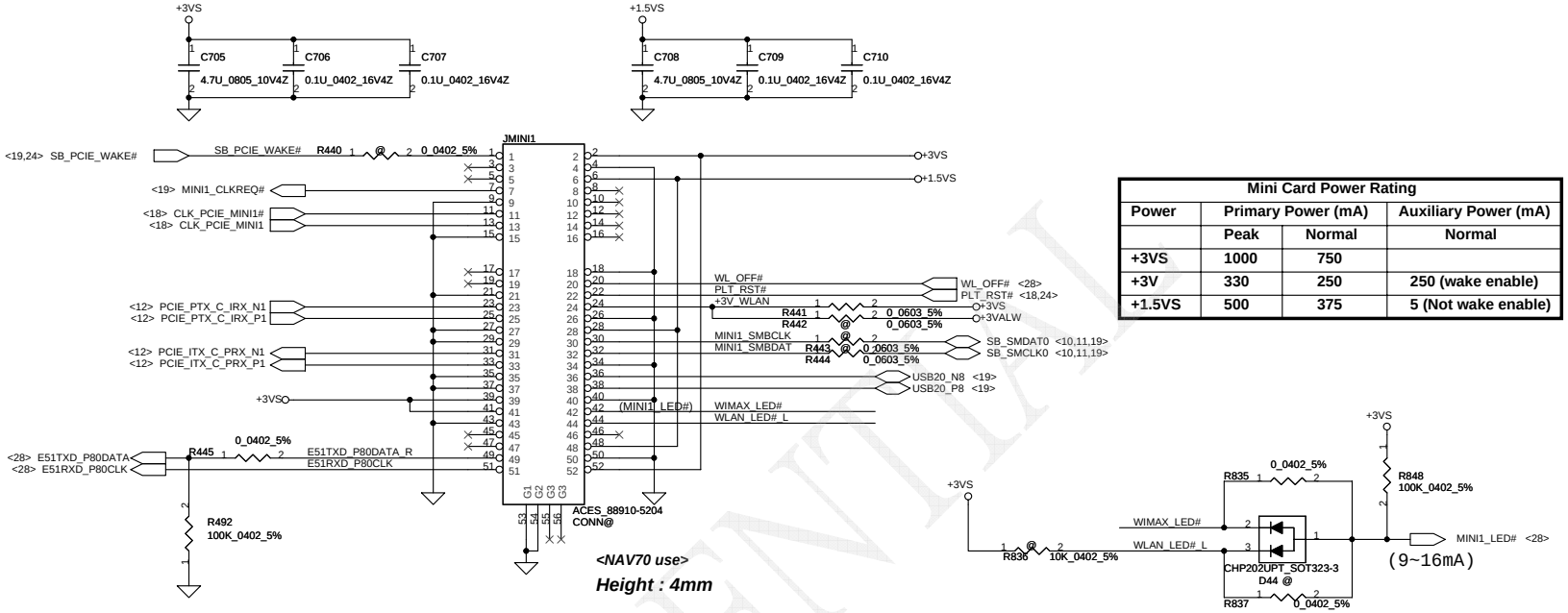
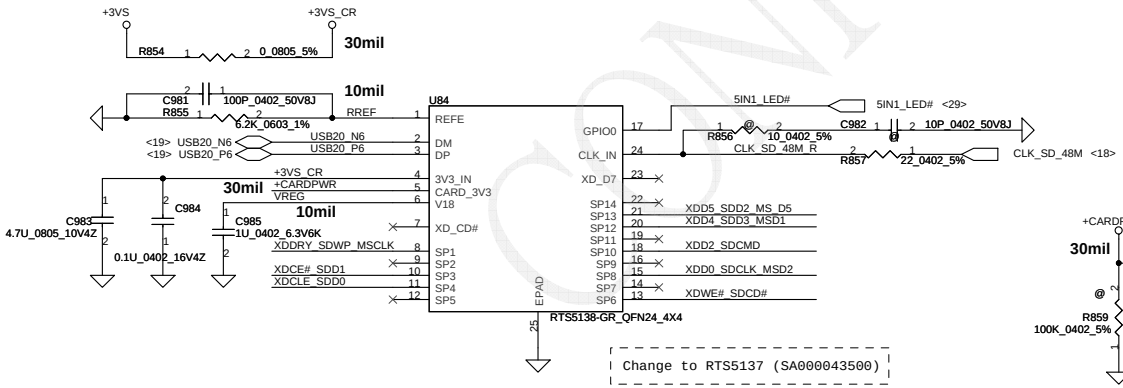
Mini-Express Card for WLAN

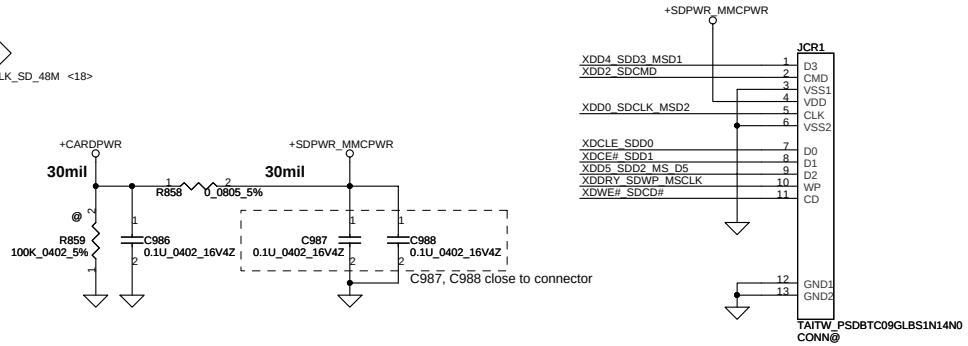


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Card Reader RTS5138 / RTS5137
(only SD+MMC function)



Card Reader Connector



Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/10/12

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Compal Electronics, Inc.

Title: MINI CARD / CardReader RTS5137

Size: B | Document Number: PEW/76/86/96 LA-6552P | Rev: B

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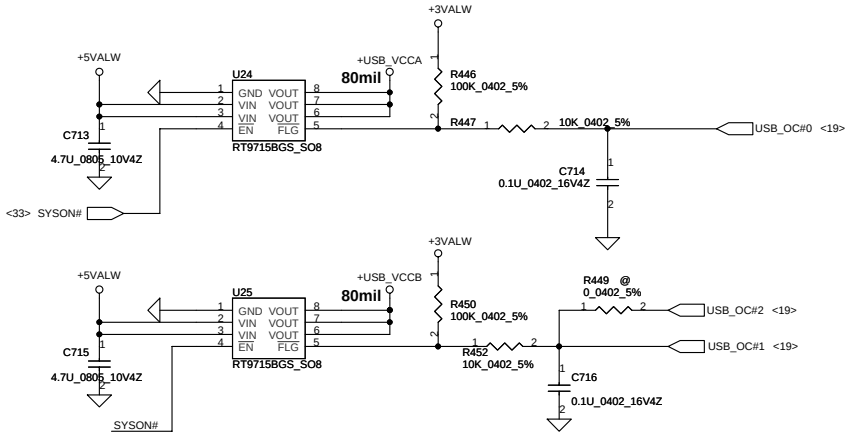
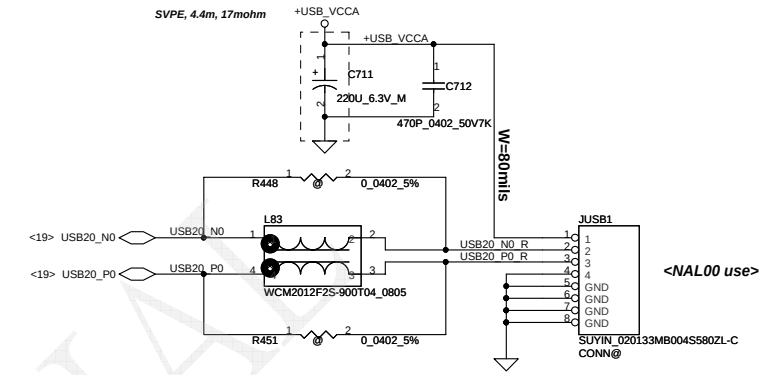
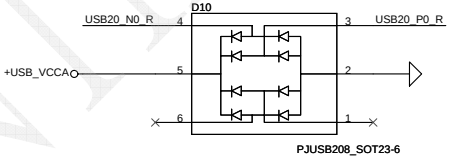
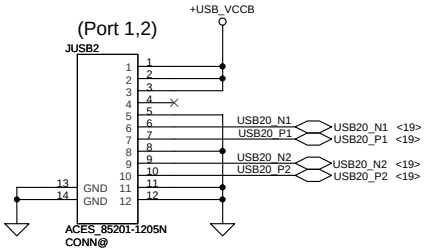






ESD Change P/N SC300000B00 For DVT

To USB/B Connector



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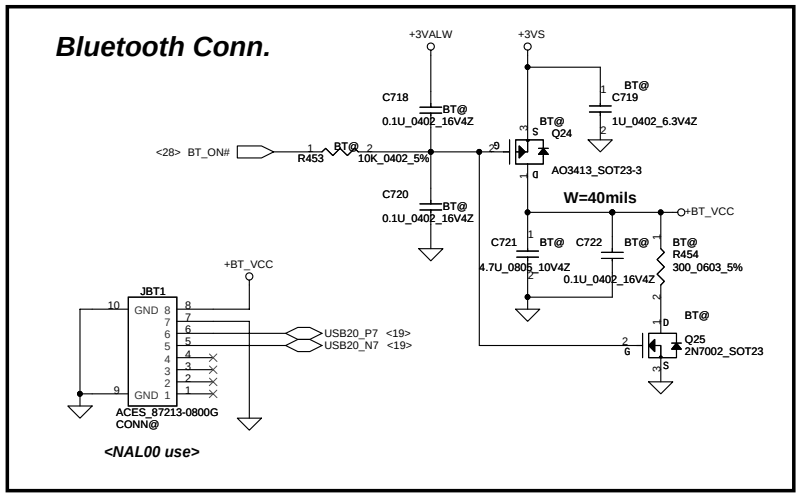

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Issued Date	2010/04/12	Deciphered Date	2010/10/12	Title: BlueTooth / Int USB x2 /eSATA
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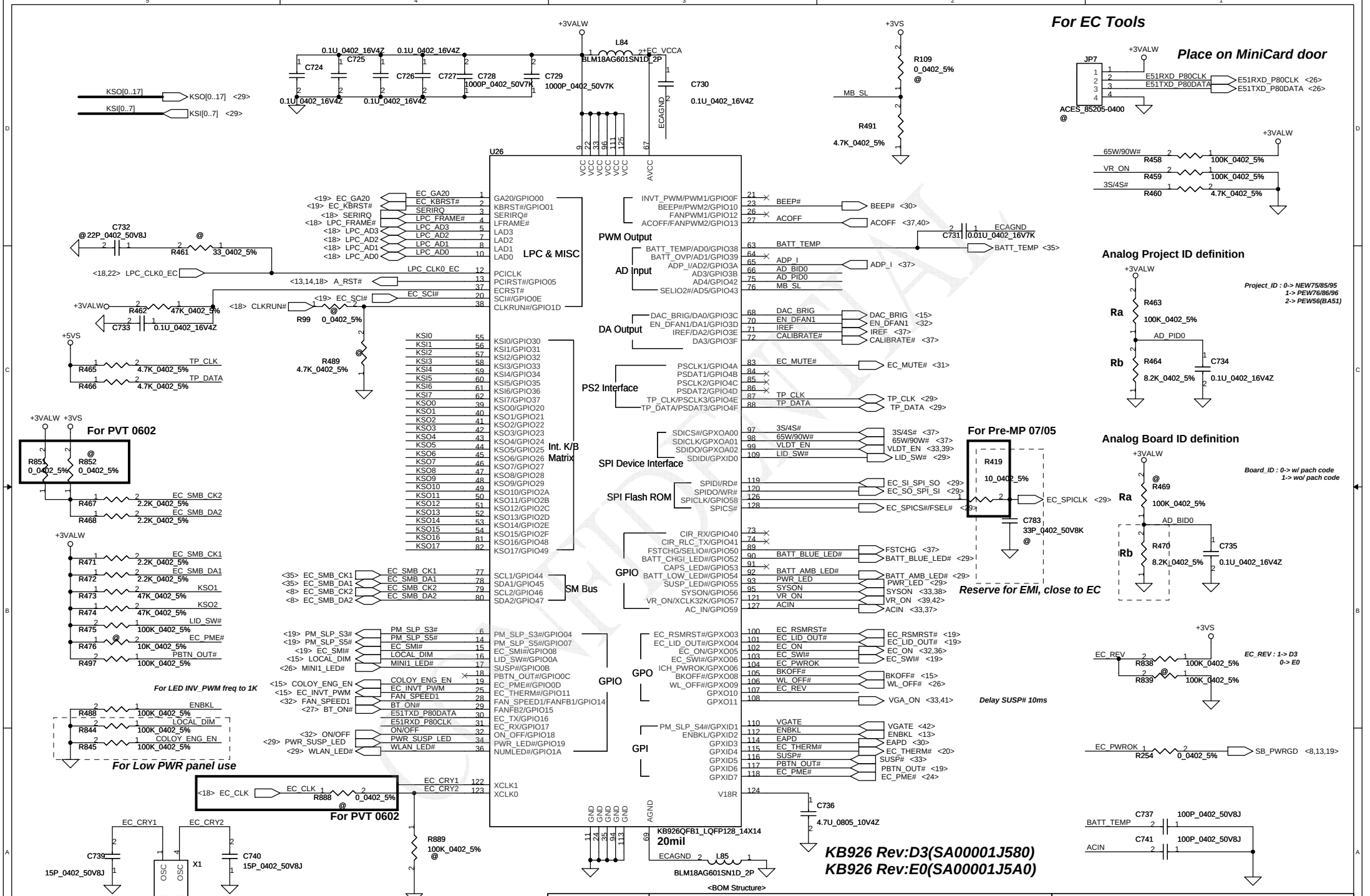

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Compal Electronics, Inc.

Title: EC ENE KB926

Size: B | Document Number: PEW/76/86/96 LA-6552P | Rev: B

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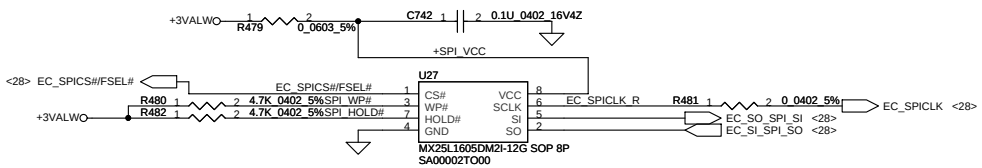
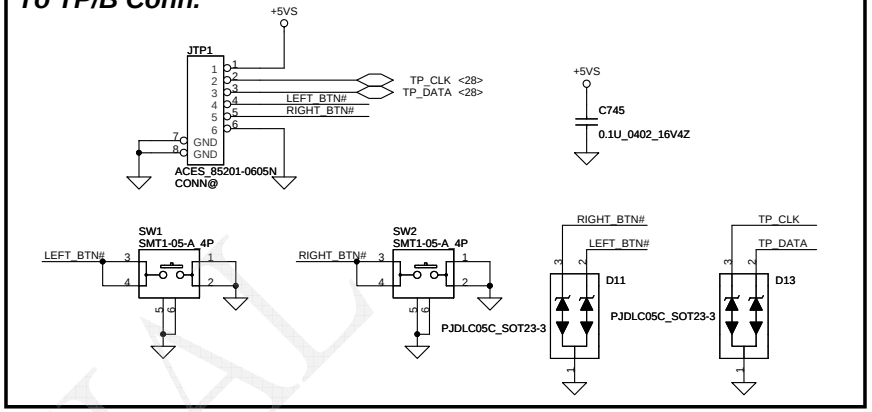
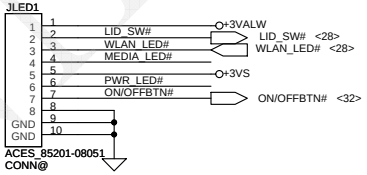
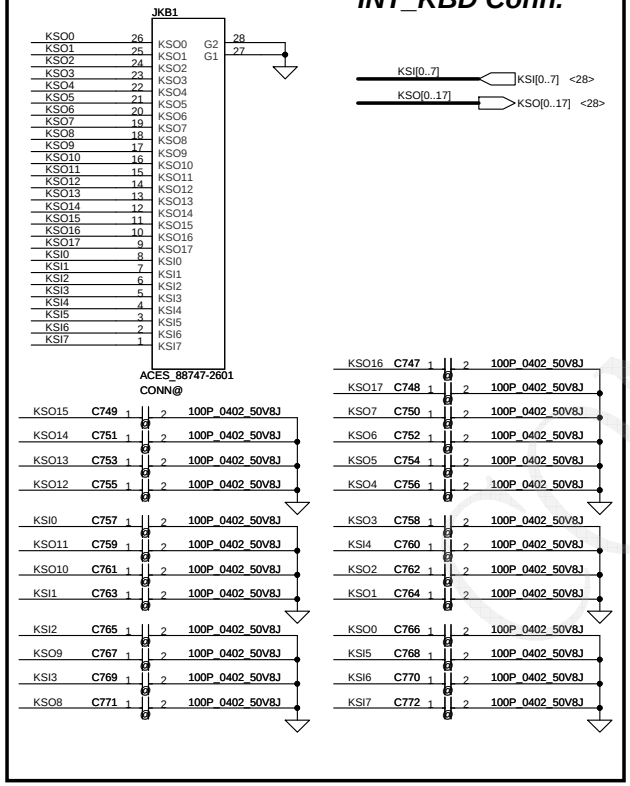


To TP/B Conn.

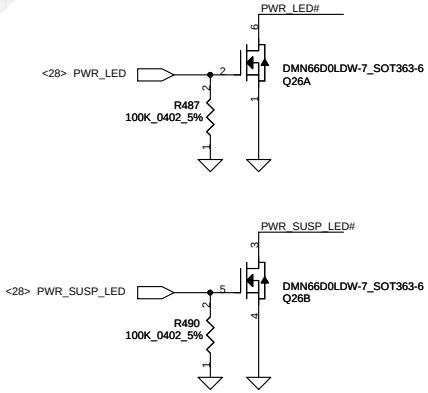




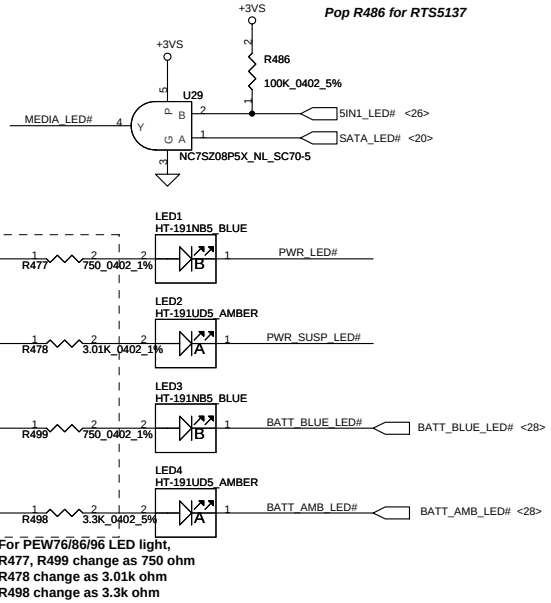
INT_KBD Conn.



For PVT 0608 Unpop Cap.



Pop R486 for RTS5137



For PEW76/86/96 LED light,
R477, R499 change as 750 ohm
R478 change as 3.01k ohm
R498 change as 3.3k ohm

Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2010/04/12	Deciphered Date	2010/10/12	Title: BIOS, I/O Port & K/B Connector
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				Date: Thursday, July 22, 2010 — Sheet 29 of 45

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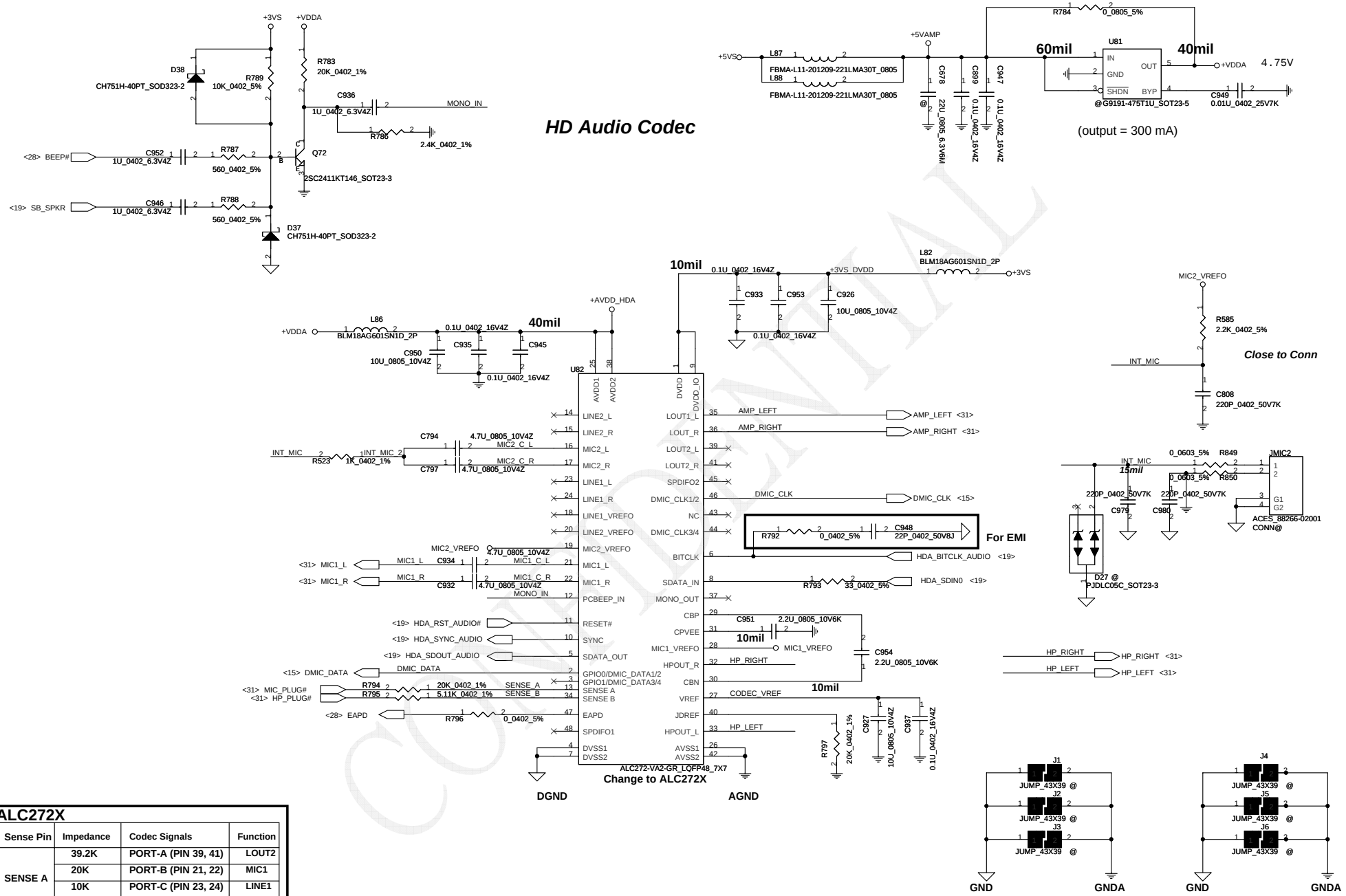

ALC272X

Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	LOUT2
	20K	PORT-B (PIN 21, 22)	MIC1
	10K	PORT-C (PIN 23, 24)	LINE1
	5.1K	PORT-D (PIN 35, 36)	LOUT1
SENSE B	39.2K	PORT-E (PIN 14, 15)	LINE2
	20K	PORT-F (PIN 16, 17)	MIC2
	10K		
	5.1K	PORT-I (PIN 32, 33)	HP

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Compal Electronics, Inc.

Title: HD Audio Codec ALC272X

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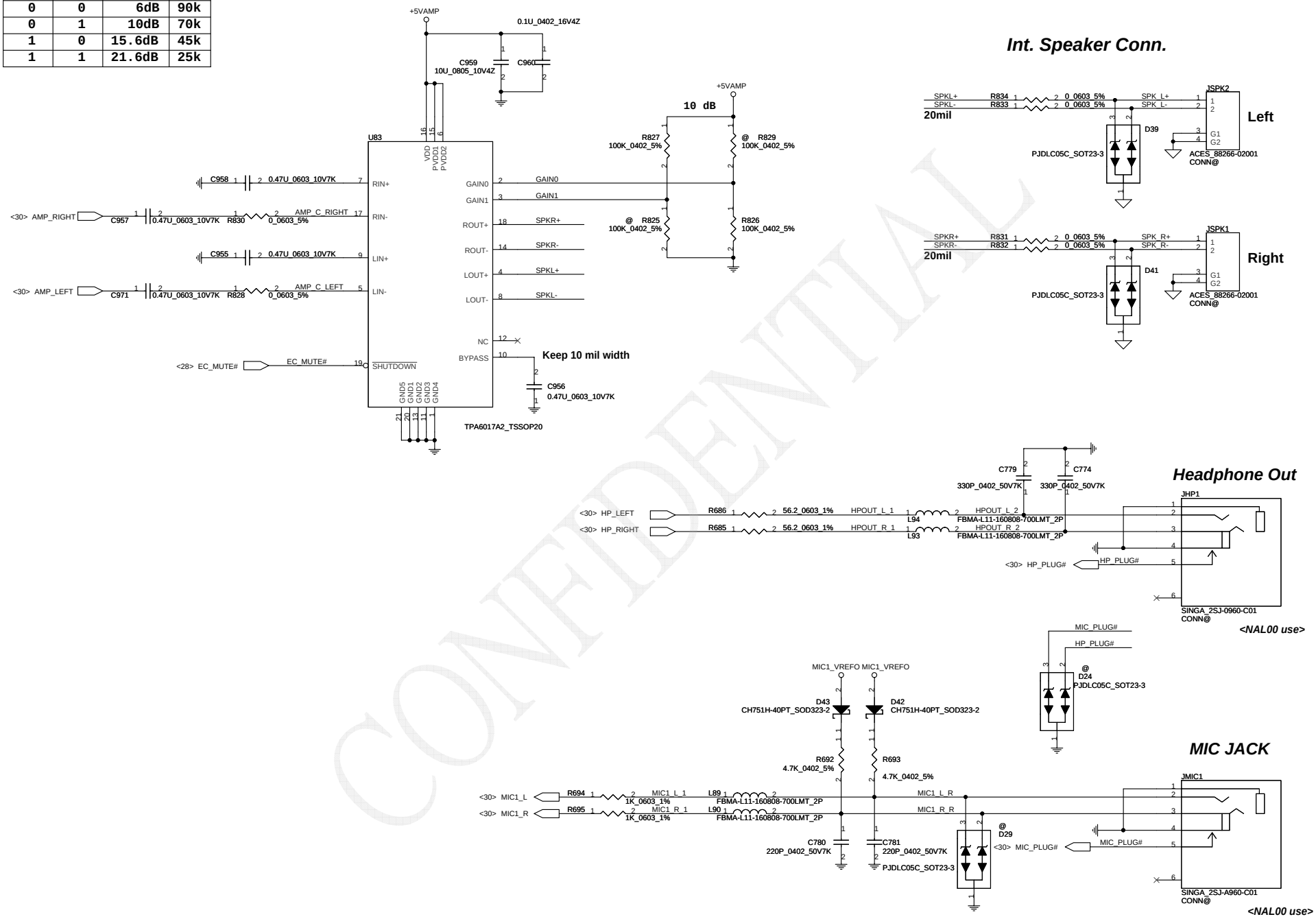
GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k



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Issued Date	2010/04/12	Deciphered Date	2010/10/12	Title: Amplifier & Audio Jack
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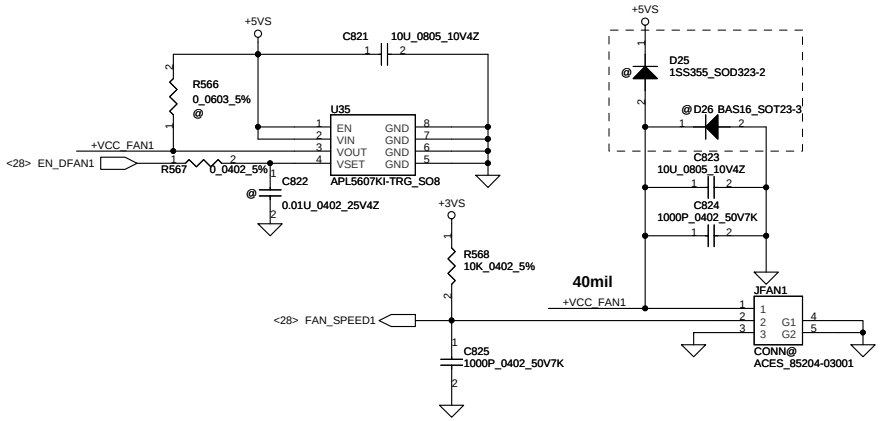
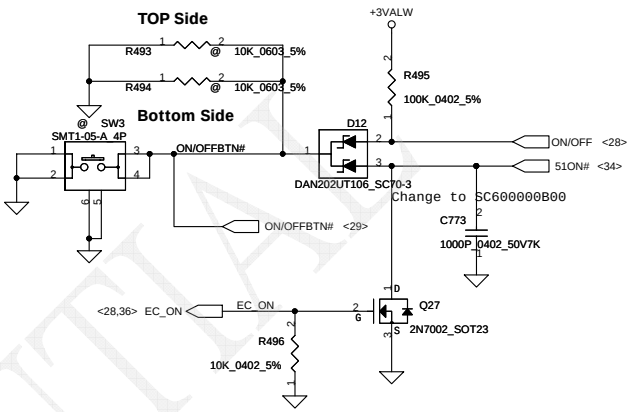
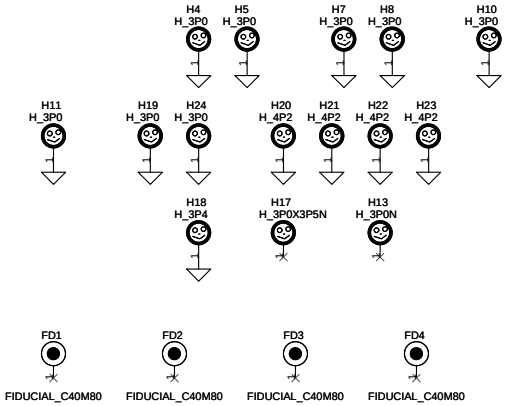
FAN1 Conn



ON/OFF switch ***Power Button***





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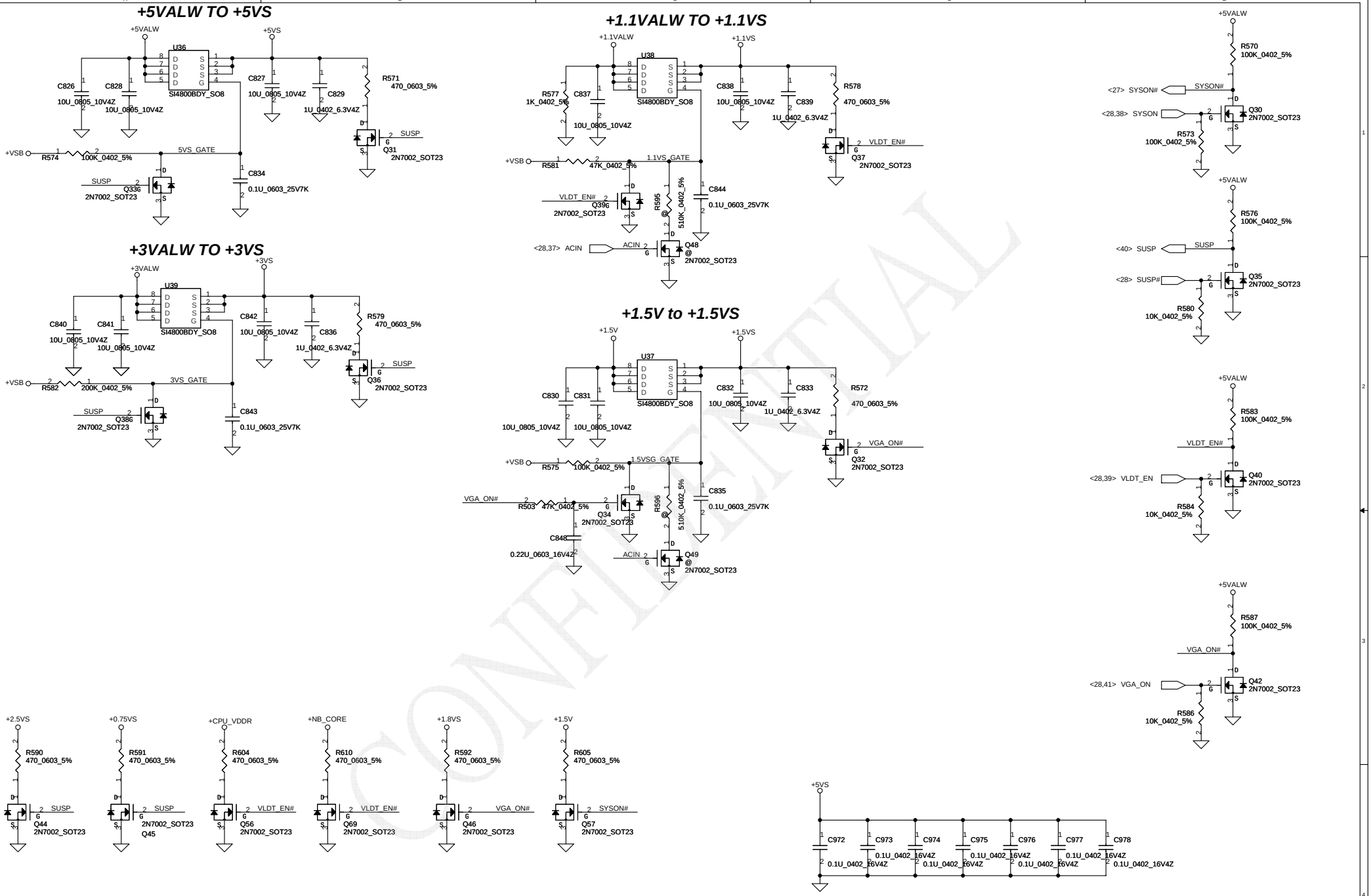

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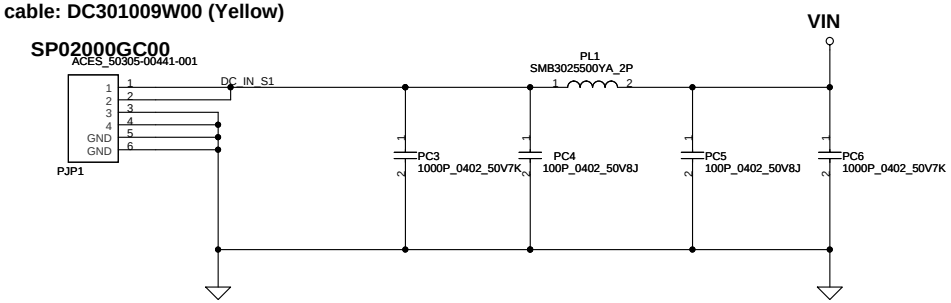
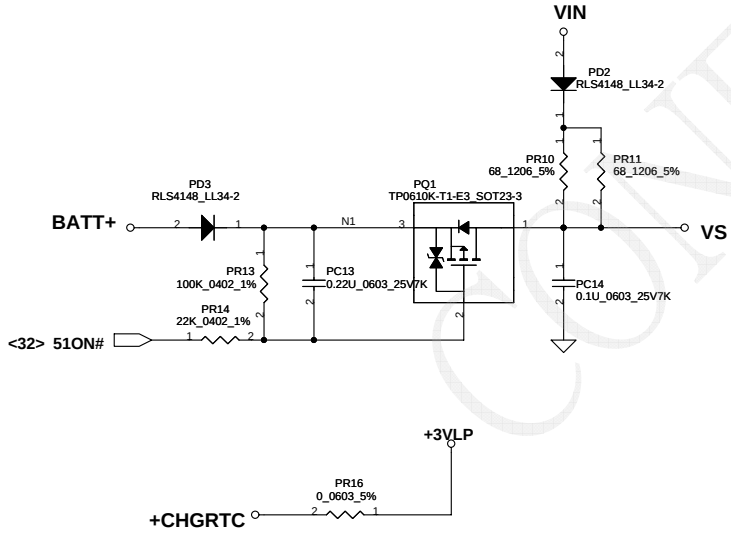
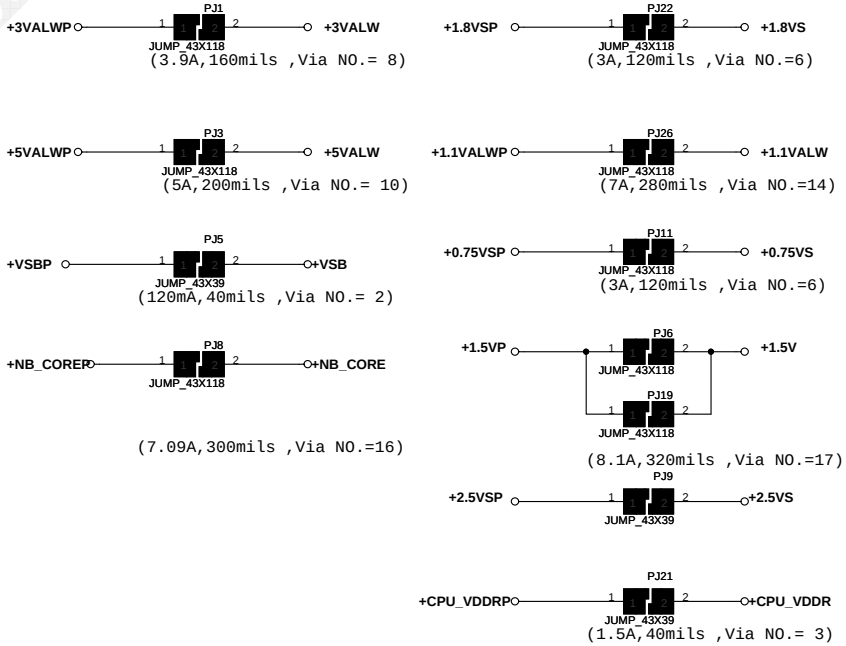
DC-IN cable: DC301009W00 (Yellow)







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Compal Electronics, Inc.

Title: DCIN & DETECTOR

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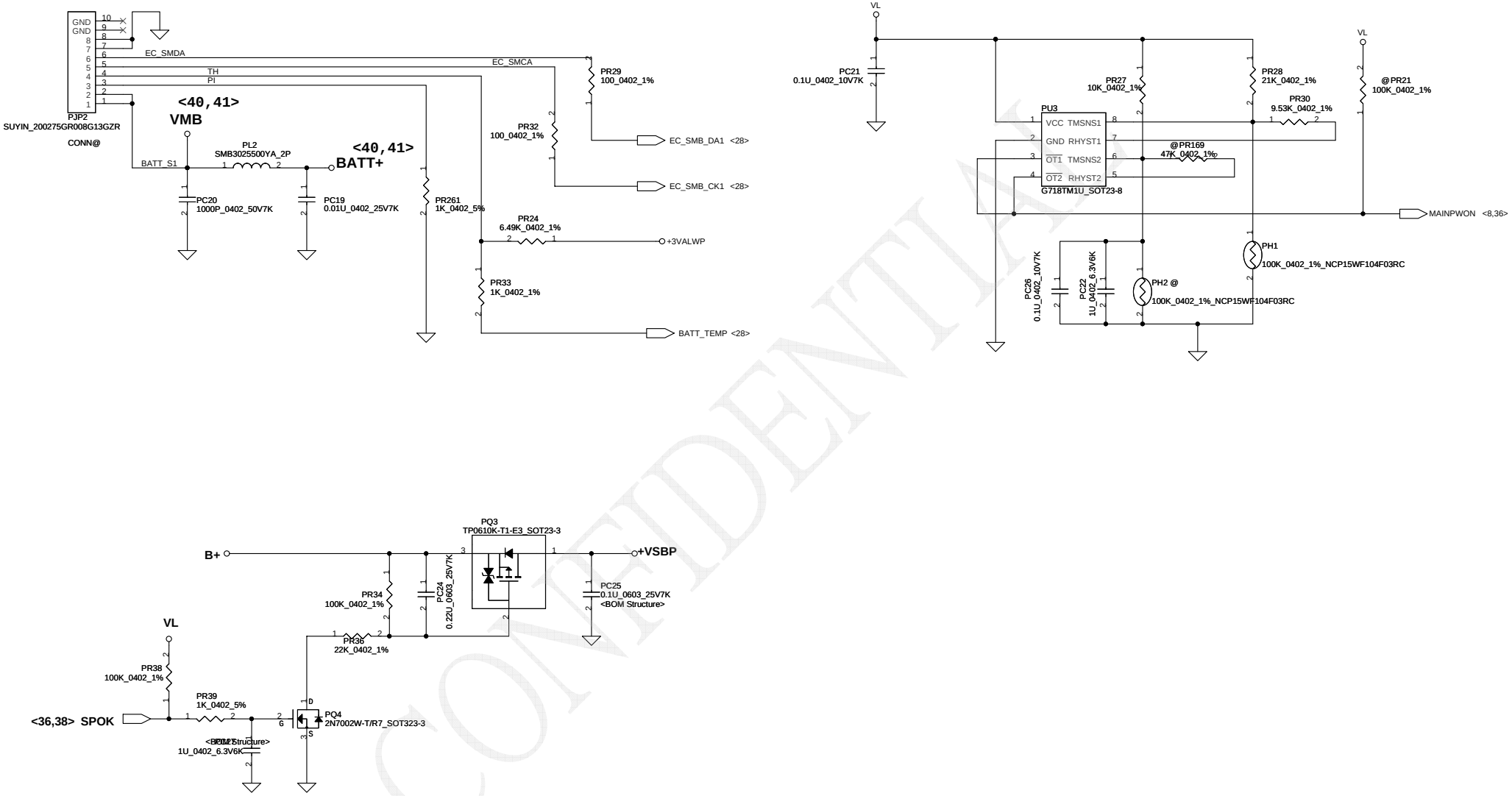
PH1 under CPU botten side : Not SPEC, reference only!
CPU thermal protection at 92 degree C
Recovery at 56 degree C



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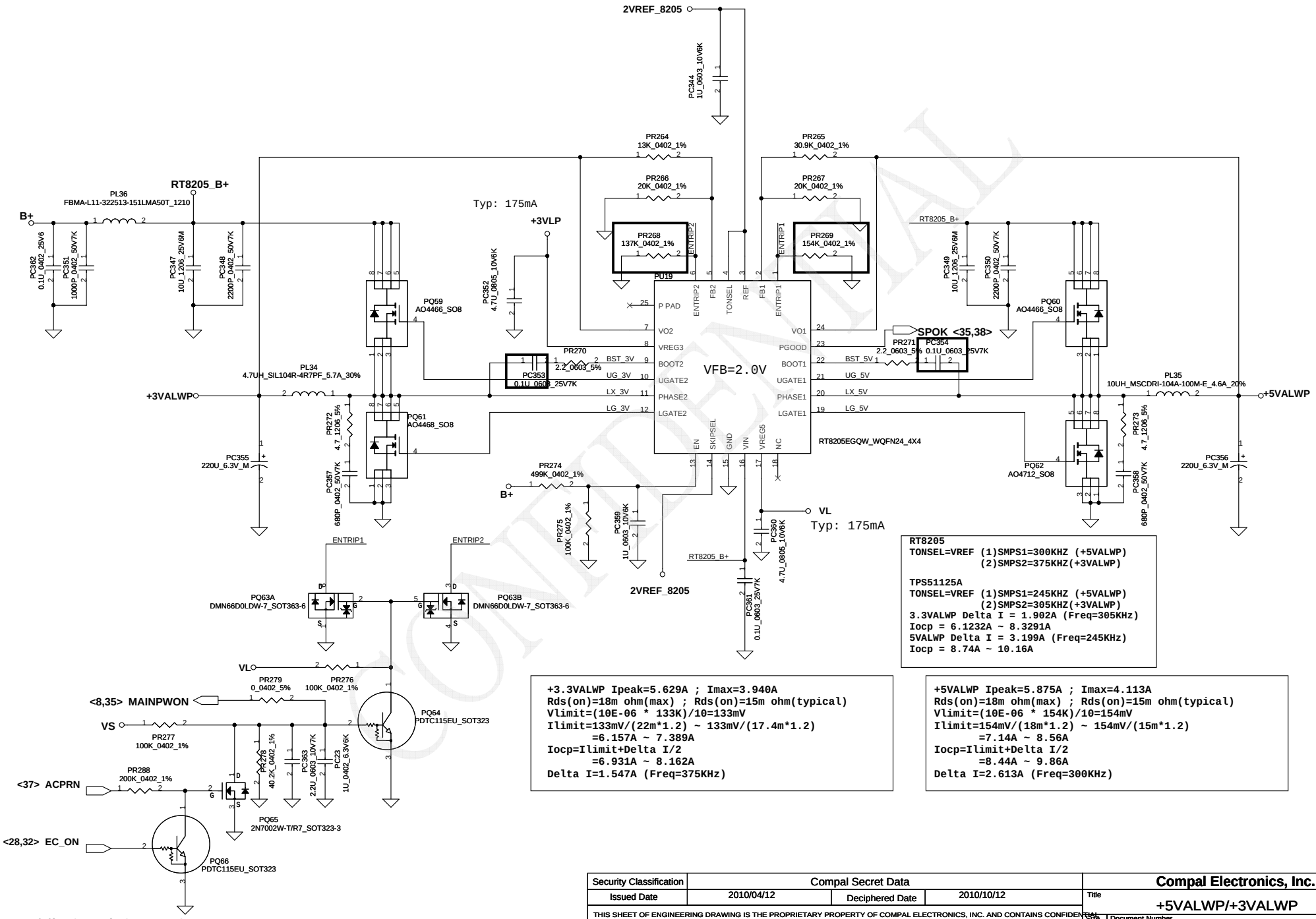
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



RT8205
TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)
(2)SMPS2=375KHZ(+3VALWP)

TPS51125A
TONSEL=VREF (1)SMPS1=245KHZ (+5VALWP)
(2)SMPS2=305KHZ(+3VALWP)
3.3VALWP Delta I = 1.902A (Freq=305KHz)
Iocp = 6.1232A ~ 8.3291A
5VALWP Delta I = 3.199A (Freq=245KHz)
Iocp = 8.74A ~ 10.16A

+3.3VALWP Ipeak=5.629A ; Imax=3.940A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(10E-06 * 133K)/10=133mV
Ilimit=133mV/(22m*1.2) ~ 133mV/(17.4m*1.2)
=6.157A ~ 7.389A
Iocp=Ilimit+Delta I/2
=6.931A ~ 8.162A
Delta I=1.547A (Freq=375KHz)

+5VALWP Ipeak=5.875A ; Imax=4.113A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(10E-06 * 154K)/10=154mV
Ilimit=154mV/(18m*1.2) ~ 154mV/(15m*1.2)
=7.14A ~ 8.56A
Iocp=Ilimit+Delta I/2
=8.44A ~ 9.86A
Delta I=2.613A (Freq=300KHz)

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Compal Electronics, Inc.

Title: +5VALWP/+3VALWP

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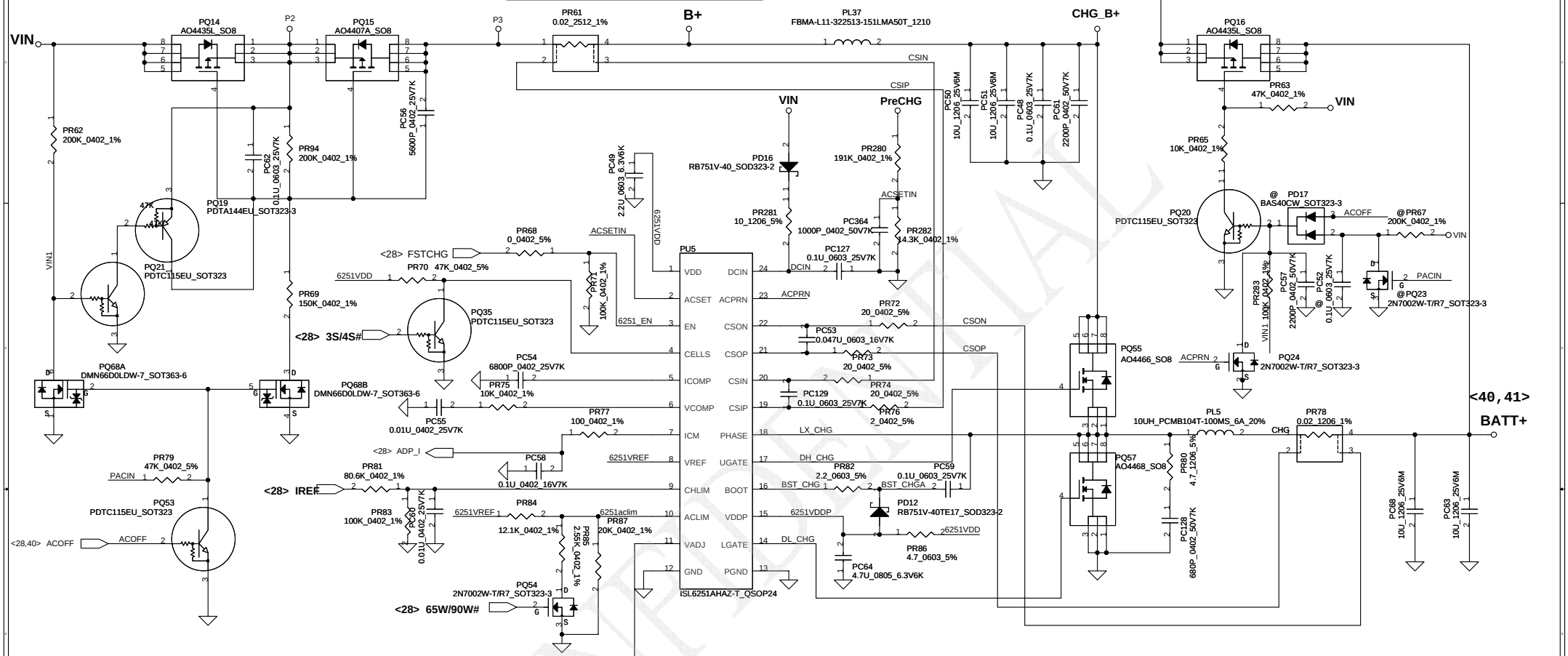
Iada=0~3.42A(65W/19V=3.421A)
Iada=0~4.74A(90W/19V=4.736A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 2.91A
CP = 85%*Iada ; CP = 4.07A



Iada=0~4.74A(90W) CP= 85%*Iada; CP=4.03A
Iada=0~3.42A(65W) CP= 85%*Iada; CP=2.91A

CP mode

Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.464V (90W), Iinput=4.03A
PR84=12.1K;PR87=20K
where Vaclm=0.391(65W), Iinput=2.91A
PR84=12.1K;PR85=2.55K

CC=0.6~4.48A

IREF=1.016*Icharge

IREF=0.43V~3.24V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

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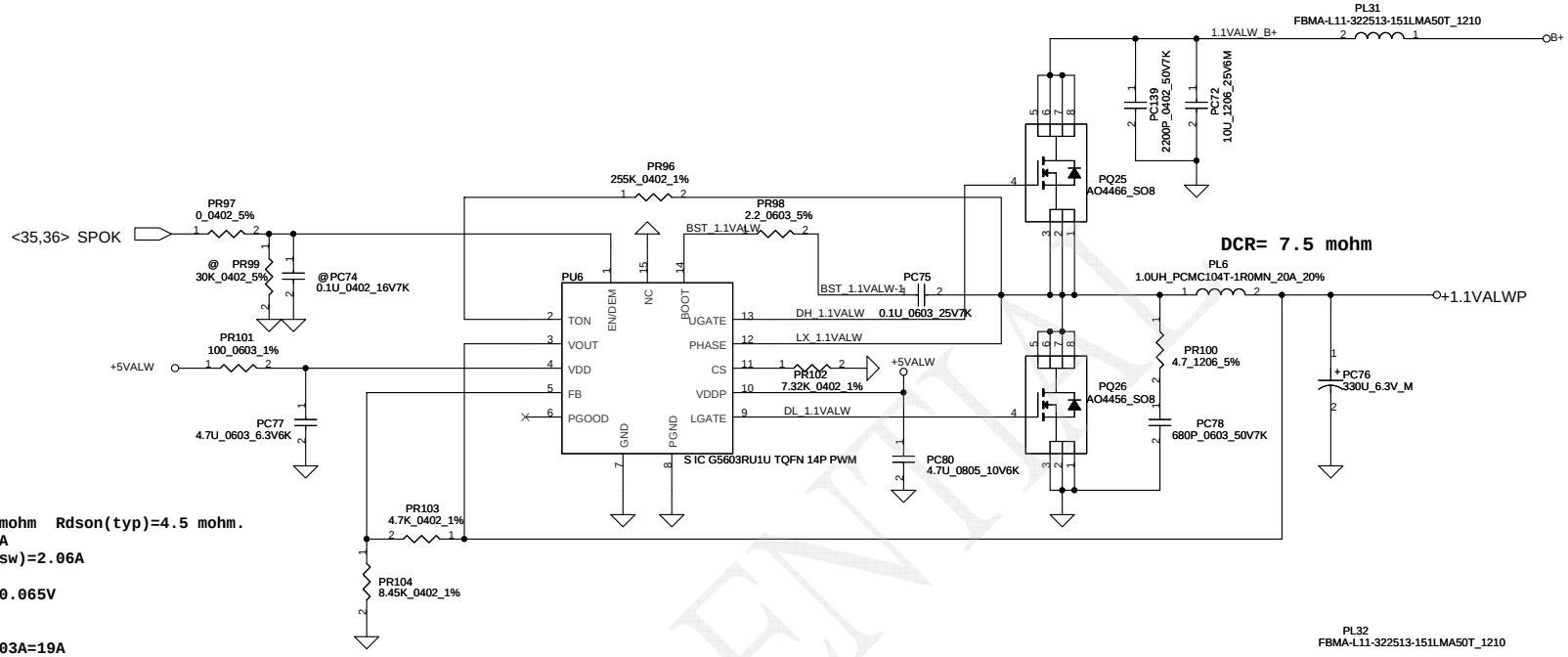
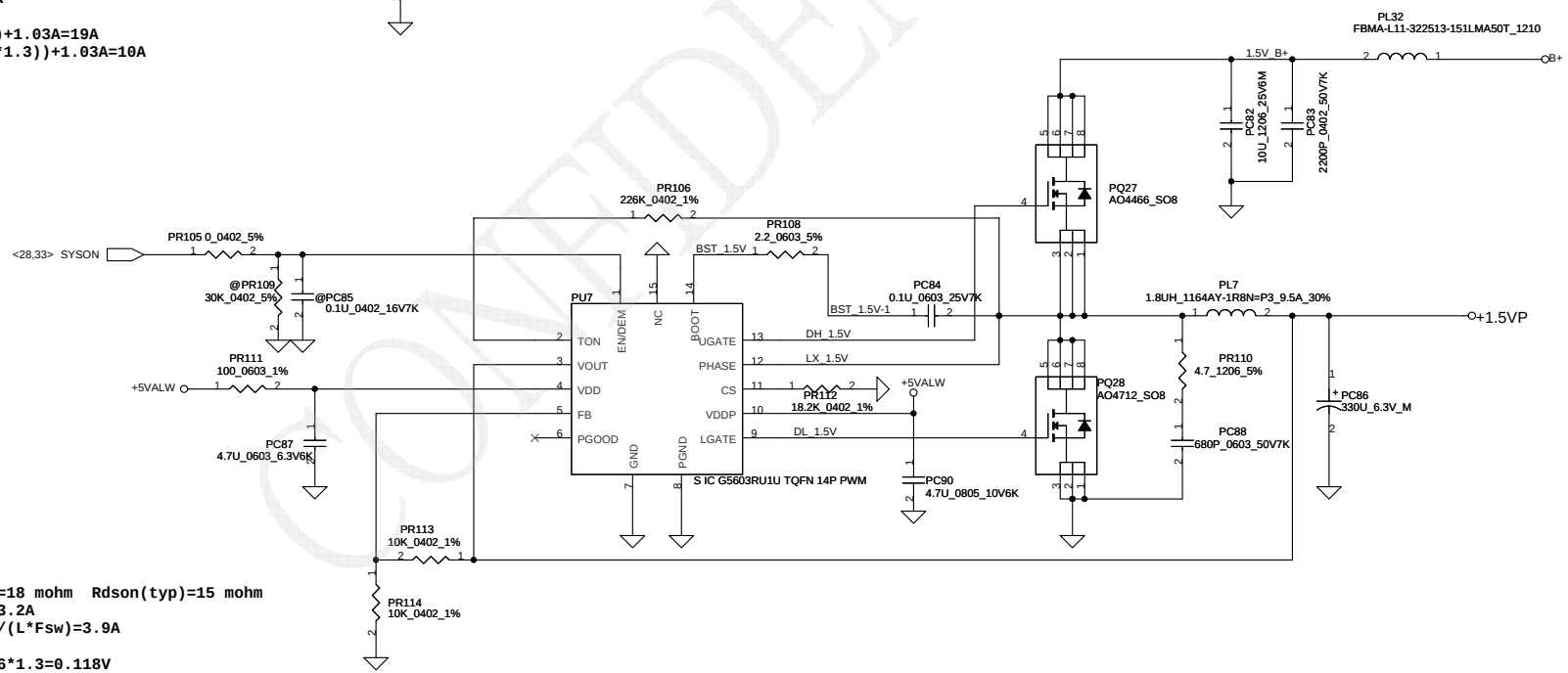


<Vo=1.1V> VFB=0.75V
V=0.75*(1+4.7K/10K)=1.1V
Fsw=280KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=7.42A, Imax=5.2A, Iocp=8.9A
Delta I=((19-1.1)*(1.1/19))/(L*Fsw)=2.06A
=>1/2Delta I=1.03A
Vtripmax=Iocp*Rdson=8.9*5.6*1.3=0.065V
Rcs=Vtrip/9uA=0.065V/9uA=7.2K
choose Rcs=7.32K
Iocpmax=((7.32K*11uA)/0.0045)+1.03A=19A
Iocpmin=((7.32K*9uA)/(0.0056*1.3))+1.03A=10A
Iocp=10A~19A



<Vo=1.5V> VFB=0.75V
Vo=0.75*(1+10K/10K)=1.5V
Fsw=335KHz

Cout ESR=17 mohm Rdson(max)=18 mohm Rdson(typ)=15 mohm
Ipeak=7A, Imax=8.4A, Iocp=13.2A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=3.9A
=>1/2Delta I=1.95A
Vtripmax=Iocp*Rdson=16.2*5.6*1.3=0.118V
Rcs=Vtrip/9uA=0.118V/9uA=13.1K
choose Rcs=13K
Iocpmax=((13K*11uA)/0.0045)+1.95A=32A
Iocpmin=((13K*9uA)/(0.0056*1.3))+1.95A=18A
Iocp=9.94A~13.2A

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Issued Date	2010/04/12	Deciphered Date	2010/10/12	Title: 1.1VALWP/1.5VP

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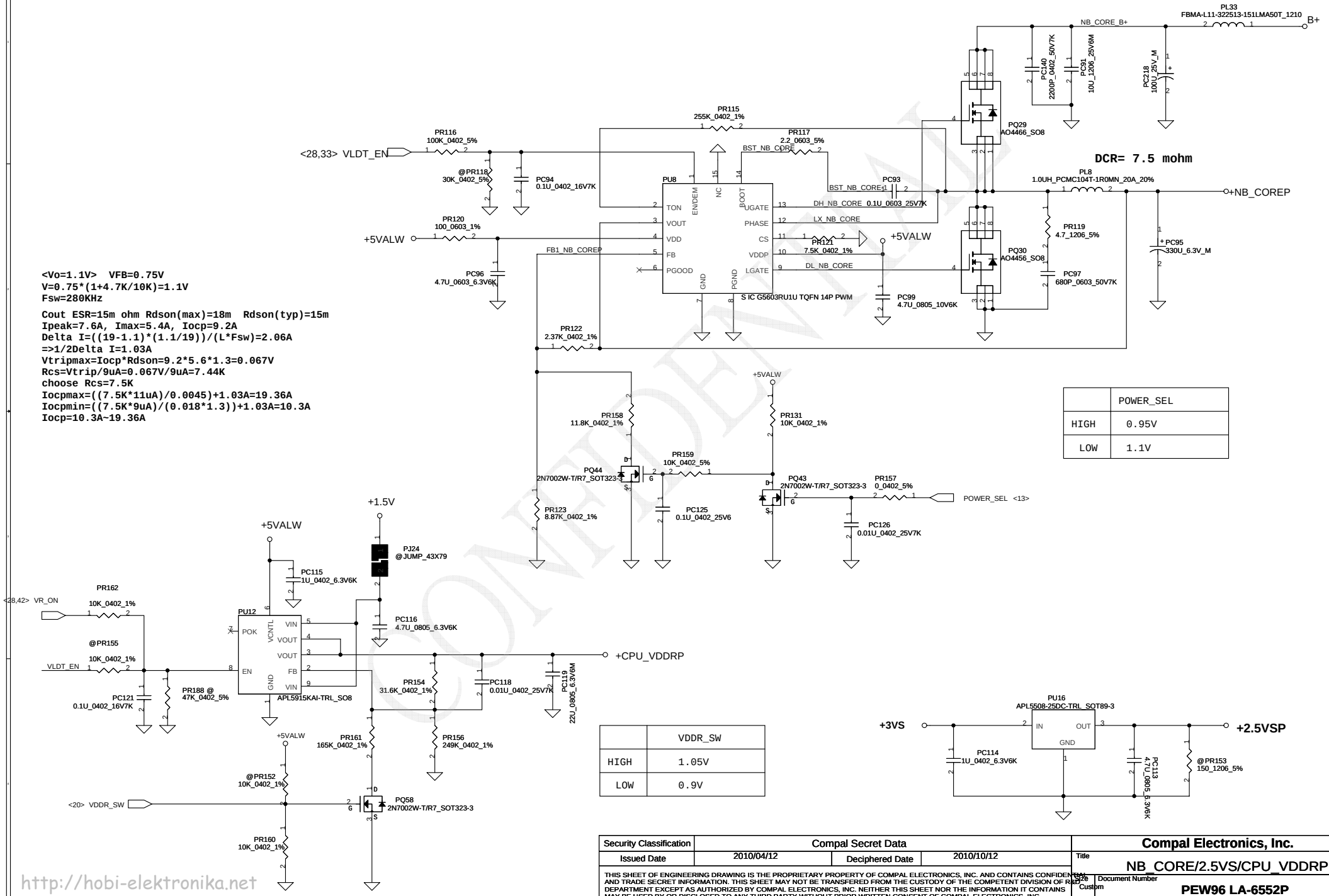

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Compal Electronics, Inc.

Title: NB_CORE/2.5VS/CPU_VDDRP

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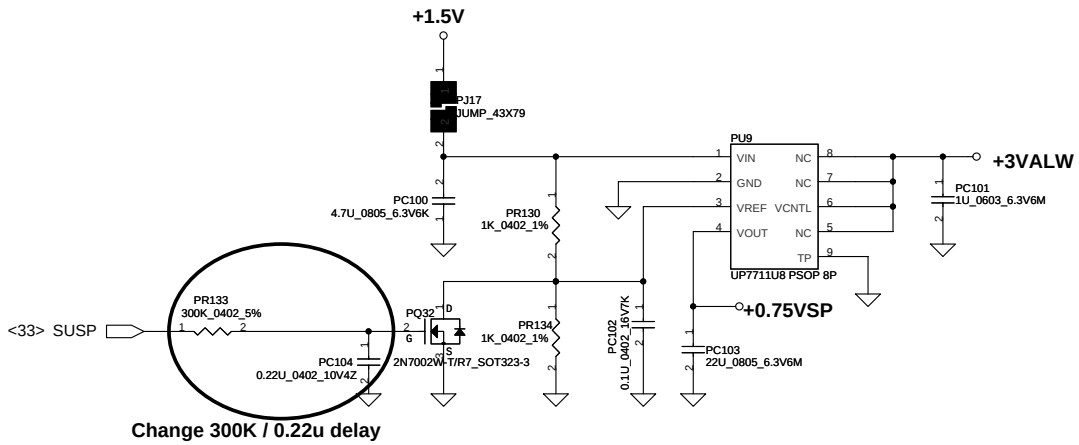
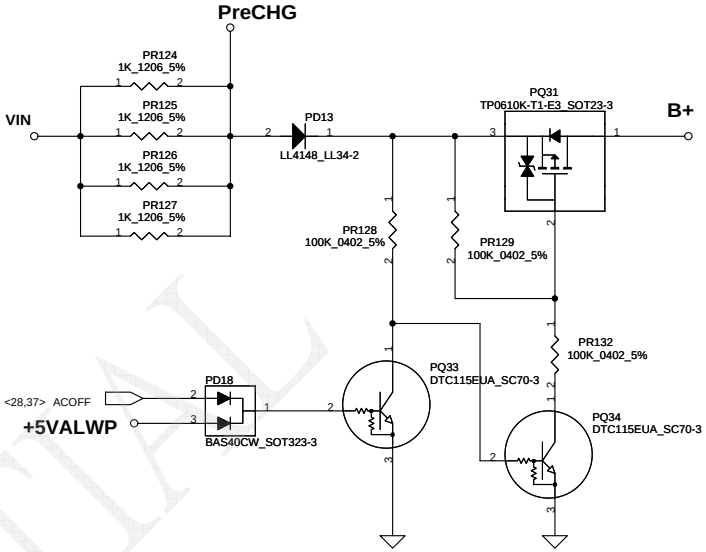


Ipeak=1A, Imax=0.7A



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				Date: Thursday, July 22, 2010; Sheet 40 of 45

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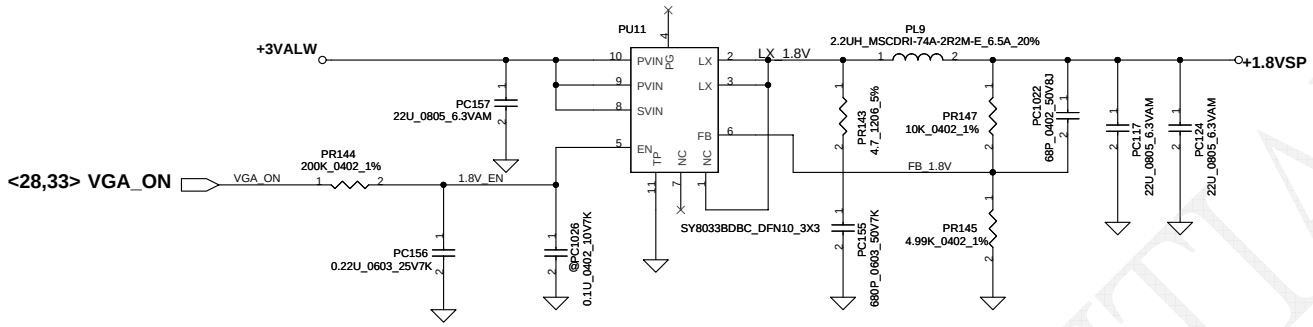
FB=0.6V
Note:Iload(max)=3.5A



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Title: +1.8VSP

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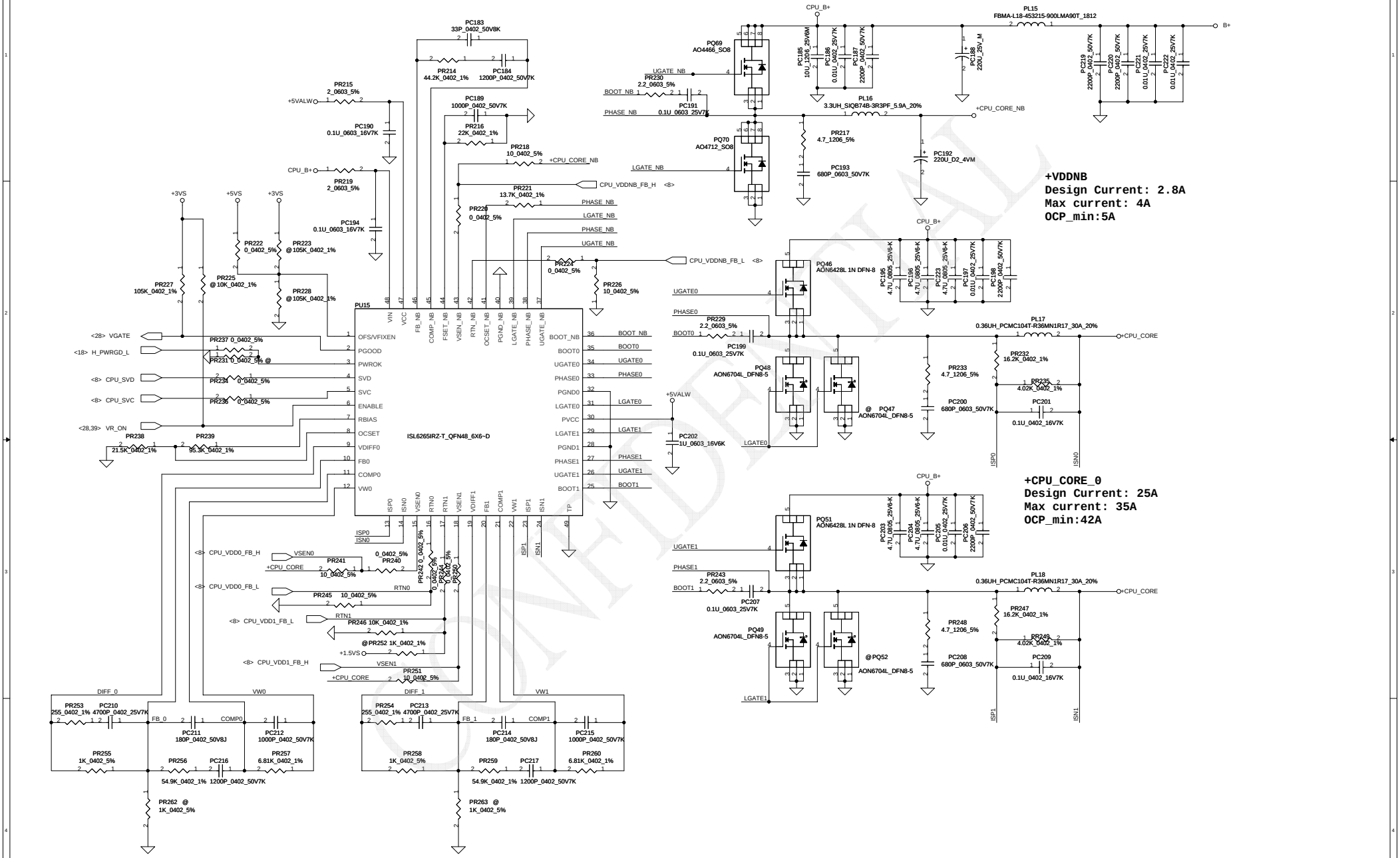

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C	NAV71	B

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Modify Pre-charger				Add PR279,PR288,PC57 Change PR285 100K to 47K Change PR287 20K to 14.3K Change PQ67 2N7002 to PDTC115 Change PR62 47K to 200K Change PR79 22K to47K Change PR283 0 to 100K	2010 0528	PVT
2	Meet common rule				Change PJ30 to PL36, PJ23 to PL37 Add PC361,PC362	2010 0602	PVT
3	HDMI test fail	5V voltage too low at test termial		36	Change PR265 from 30K to 30.9K	2010 0604	PVT
4	ESD test fail	ESD solution			Add PC22, PC23	2010 0608	PVT
5	EMI test fail	EMI solution			Enable 3V,5V,1.1V,1.5V,NB_CORE,CPU snubber	2010 0608	PVT
6	Power sequence tune			41	Change PR144 from 22K to 200K Change PC156 from 0.47u to 0.22u	2010 0609	PVT
7	Costdown	Costdown		38	Change PQ28 from AO4456 to AO4712 Change PR112 from 13K to 18.2K Change PL7 from 1.0uH to 1.8uH Change PQ61 from AO4712 to AO4468	2010 0617	PVT
8					PR268 from 133K to 137K PQ57 from AO4466 to AO4468		
9	For DDR voltage default/HW YC	DDR 2 need 0.9V, DDR 3 need 1.05V But DDR2 voltage is critical then DDR 3		39	Disable PR152 Enable PR160	2010 0705	Pre MP
10	Aprove 200MHz~220MHz/EMI Chris	EMI solution		37	Enable PR80, PC128 Change PR82 from 0 to 2.2	2010 0705	Pre MP
11	Add a bypass path/ESD Chris	ESD solution		35	Add PC26 near PC22	2010 0705	Pre MP
12							
13							
14							
15							
16							

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Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: PEW96 LA-6552P | Rev: B

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							

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Compal Electronics, Inc.

Title: PIR (PWR)

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05/10 First release

1. Change Cardreader chip (RTS5137/RTS5138)
2. ODD used to ODD sub/b
3. RTC Battery change (w/o charge)

06/11 PVT

1. P.28 Reserve R889 For EC_CLK, pop R851, unpop R852 For EC_SMBus leakage
2. P.26 Remove R853
3. P.28 project ID-->1 Board ID -->1, unstuff KSI, KSO Cap.
4. P.8 Change R41 as 31.6k ohm and R42 as 30k ohm for TSI

07/05 Pre-MP

1. P.19 Reserve R890 For MEM_1V5
2. P.28 Change R419 as 10 ohm For EMI

07/20

1. P.29 Change R477, R499 as 750 ohm; change R478 as 3.01k ohm; change R498 as 3.3k ohm for LED light

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Compal Electronics, Inc.

Title: HW PIR

Size: B | Document Number: PEW/76/86/96 LA-6552P | Rev: B

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